**Features**

- Ballast control and half-bridge driver in one IC
- Transformer-less lamp power sensing
- Closed-loop lamp power control
- Closed-loop preheat current control
- Programmable preheat time
- Programmable preheat current
- Lamp ignition detection
- Programmable ignition-to-dim time
- 0.5 to 5VDC dimming control input
- Min and max lamp power adjustments
- Programmable minimum frequency
- Internal current sense blanking
- Full lamp fault protection
- Brown-out protection
- Automatic restart
- Micro-power startup
- Zener clamped Vcc
- Over-temperature protection
- 16-pin DIP and SOIC package types

**Description**

Description: The IR21592/IR21593 are complete dimming ballast controllers and 600V half-bridge drivers all in one IC. The architecture includes phase control for transformer-less lamp power sensing and regulation which minimizes changes needed to adapt non-dimming ballasts for dimming. Externally programmable features such as preheat time and current, ignition-to-dim time, and a complete dimming interface with minimum and maximum settings provide a high degree of flexibility for the ballast design engineer. Protection from failure of a lamp to strike, filament failures, thermal overload, or lamp failure during normal operation, as well as an automatic restart function, have been included in the design. The heart of this control IC is a voltage-controlled oscillator with externally programmable minimum frequency. The IR21592/IR21593 are available in both 16 pin DIP and 16 pin narrow body SOIC packages.

**Typical Connection**

![Typical Connection Diagram](image)

**Data Sheet No. PD60194**

**IR21592(S)**

**IR21593(S)**

**Packages**

- 16 Lead SOIC (narrow body)
- 16 Lead PDIP

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## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_B)</td>
<td>High side floating supply voltage</td>
<td>-0.3</td>
<td>625</td>
<td>V</td>
</tr>
<tr>
<td>(V_S)</td>
<td>High side floating supply offset voltage</td>
<td>(V_B - 25)</td>
<td>(V_B + 25)</td>
<td></td>
</tr>
<tr>
<td>(V_{HO})</td>
<td>High side floating output voltage</td>
<td>(V_S - 0.3)</td>
<td>(V_S + 0.3)</td>
<td></td>
</tr>
<tr>
<td>(V_{LO})</td>
<td>Low side output voltage</td>
<td>-0.3</td>
<td>(V_{CC} + 0.3)</td>
<td></td>
</tr>
<tr>
<td>(I_{OMAX})</td>
<td>Maximum allowable output current (either output) due to external power transistor miller effect</td>
<td>-500</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>(V_{VCO})</td>
<td>Voltage controlled oscillator input voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>(I_{CPH})</td>
<td>CPH current</td>
<td>-5</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>(V_{IPH})</td>
<td>IPH voltage</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{DIM})</td>
<td>Dimming control pin input voltage</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{MAX})</td>
<td>Maximum lamp power setting pin input voltage</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{MIN})</td>
<td>Minimum lamp power setting pin input voltage</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CS})</td>
<td>Current sense input voltage</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(I_{SD})</td>
<td>Shutdown pin current</td>
<td>-5</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Supply current (note 1)</td>
<td>—</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>(dV/dt)</td>
<td>Allowable offset voltage slew rate</td>
<td>-50</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>(P_D)</td>
<td>Package power dissipation @ (T_A \leq 25^\circ C)</td>
<td>—</td>
<td>1.60</td>
<td>W</td>
</tr>
<tr>
<td>(P_D = (T_{JMAX} - T_A)/R_{thJA})</td>
<td>(16 pin DIP)</td>
<td>—</td>
<td>1.25</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{thJA})</td>
<td>Thermal resistance, junction to ambient</td>
<td>—</td>
<td>75</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{thJA})</td>
<td>(16 pin SOIC)</td>
<td>—</td>
<td>115</td>
<td>°C/W</td>
</tr>
<tr>
<td>(T_J)</td>
<td>Junction temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_S)</td>
<td>Storage temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_L)</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>—</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note 1:** This IC contains a zener clamp structure between the chip \(V_{CC}\) and COM which has a nominal breakdown voltage of 15.6V (\(V_{CLAMP}\)). Please note that this supply pin should not be driven by a DC, low impedance power source greater than the diode clamp voltage (\(V_{CLAMP}\)) as specified in the Electrical Characteristics section.
Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

### Symbol | Definition | Min. | Max. | Units | Test Conditions
--- | --- | --- | --- | --- | ---
V<sub>BS</sub> | High side floating supply voltage | V<sub>CC</sub> - 0.7 | V<sub>CLAMP</sub> | V | |
V<sub>S</sub> | Steady state high side floating supply offset voltage | -1 | 600 | V | |
V<sub>CC</sub> | Supply voltage | V<sub>CCUV+</sub> | V<sub>CLAMP</sub> (1.56) | V | |
I<sub>CC</sub> | Supply current | note 2 | 10 | mA | |
V<sub>VCO</sub> | VCO pin voltage | 0 | 5 | V | |
V<sub>DIM</sub> | DIM pin voltage | 0 | 5 | V | |
V<sub>MAX</sub> | MAX pin current (note 3) | -750 | 0 | µA | |
V<sub>M</sub> | MIN pin voltage | 1 | 3 | V | |
R<sub>FMIN</sub> | Minimum frequency setting resistance | 10 | 100 | kΩ | |
I<sub>SD</sub> | Shutdown pin current | -1 | 1 | mA | |
I<sub>CS</sub> | Current sensing pin current | -1 | 1 | mA | |
T<sub>J</sub> | Junction temperature | -40 | 125 | °C | |

**Note 2:** Enough current should be supplied into the VCC lead to keep the internal 15.6V zener clamp diode on this lead regulating its voltage, V<sub>CLAMP</sub>.

**Note 3:** The MAX lead is a voltage-controlled current source. For optimum dim interface current mirror performance, this current should be kept between 0 and 750µA.

**Electrical Characteristics**

V<sub>CC</sub> = V<sub>BS</sub> = V<sub>BIAS</sub> = 14V +/- 0.25V, V<sub>CS</sub> = 0.5V, V<sub>SD</sub> = 0.0V, R<sub>FMIN</sub> = 40kΩ, C<sub>VCO</sub> = 10 nF, V<sub>DIM</sub> = 0.0V, R<sub>MAX</sub> = 33kΩ, R<sub>MIN</sub> = 56kΩ, V<sub>CREF</sub> = 0.0V, C<sub>L,HO</sub> = 100pF, T<sub>A</sub> = 25°C unless otherwise specified.

### Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions
--- | --- | --- | --- | --- | --- | ---
V<sub>CCUV+</sub> | V<sub>CC</sub> supply undervoltage positive going threshold | 12.0 | 12.5 | 13.0 | V | |
V<sub>CHYS</sub> | V<sub>CC</sub> supply undervoltage lockout hysteresis | 1.5 | 1.6 | 1.7 | µA | V<sub>CC</sub> = 10V |
I<sub>QCCUV</sub> | UVLO mode quiescent current | — | 200 | — | µA | SD=5V, CS=2V, or T<sub>J</sub> > T<sub>SD</sub> |
I<sub>QCCF</sub> | Fault-mode quiescent current | — | 240 | — | µA | |
I<sub>QCCFMIN</sub> | V<sub>CC</sub> supply current @ FMIN (IR21592) | — | 5.6 | — | mA | V<sub>CC</sub> = 0V |
I<sub>QCCFMAX</sub> | V<sub>CC</sub> supply current @ MAX (IR21592) | — | 6.6 | — | mA | V<sub>CC</sub> = 5V |
I<sub>QCCFMIN</sub> | V<sub>CC</sub> supply current @ FMIN (IR21593) | — | 5.4 | — | mA | V<sub>CC</sub> = 0V |
I<sub>QCCFMAX</sub> | V<sub>CC</sub> supply current @ MAX (IR21593) | — | 6.8 | — | mA | V<sub>CC</sub> = 5V |
V<sub>CLAMP</sub> | V<sub>CC</sub> zener shunt clamp voltage | 14.5 | 15.6 | 16.5 | V | I<sub>CC</sub> = 10mA |
### Electrical Characteristics (cont.)

\[ V_{CC} = V_{BS} = V_{BIAS} = 14V \pm 0.25V, \ V_{CS} = 0.5V, \ V_{SD} = 0.0V, \ R_{FMIN} = 40k, \ C_{VCO} = 10 \text{ nF}, \ V_{DIM} = 0.0V, \ R_{MAX} = 33k, \ R_{MIN} = 56k, \ V_{TPH} = 0.0V, \ C_{LO,HO} = 1000pF, \ T_A = 25^\circ\text{C unless otherwise specified.} \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{QBS0} )</td>
<td>Quiescent ( V_{BS} ) supply current</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>( \mu \text{A} )</td>
<td>( V_{HO} = V_S )</td>
</tr>
<tr>
<td>( I_{QBS1} )</td>
<td>Quiescent ( V_{BS} ) supply current</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>( \mu \text{A} )</td>
<td>( V_{HO} = V_B )</td>
</tr>
<tr>
<td>( V_{BSMIN} )</td>
<td>Minimum required ( V_{BS} ) voltage for proper HO functionality</td>
<td>—</td>
<td>4</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{LK} )</td>
<td>Offset supply leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>( \mu \text{A} )</td>
<td>( V_B = V_S = 600V )</td>
</tr>
</tbody>
</table>

### Oscillator I/O Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{VCO} ) (IR21592)</td>
<td>VCO frequency range</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>kHz</td>
<td>( V_{VCO}=0V, \ R_{FMIN}=39K\Omega )</td>
</tr>
<tr>
<td>( f_{VCO} ) (IR21593)</td>
<td>VCO frequency range</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>kHz</td>
<td>( V_{VCO}=5V, \ R_{FMIN}=20K\Omega )</td>
</tr>
<tr>
<td>( f_{VCO} )</td>
<td>VCO frequency range (IR21593)</td>
<td>—</td>
<td>95</td>
<td>—</td>
<td>kHz</td>
<td>( V_{VCO}=0V, \ R_{FMIN}=68K\Omega )</td>
</tr>
<tr>
<td>( f_{VCO} )</td>
<td>VCO frequency range (IR21593)</td>
<td>—</td>
<td>230</td>
<td>—</td>
<td>kHz</td>
<td>( V_{VCO}=5V, \ R_{FMIN}=10K\Omega )</td>
</tr>
<tr>
<td>( I_{VCOFLT} )</td>
<td>Fault-mode VCO pin voltage (UVLO, shutdown, over-current/ temp.)</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>V</td>
<td>( V_{VCO} = 0V )</td>
</tr>
<tr>
<td>( I_{VCOPH} )</td>
<td>Preheat mode VCO pin discharge current</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>( \mu \text{A} )</td>
<td>( V_{CPH} &lt; 5V )</td>
</tr>
<tr>
<td>( I_{VCODIM} )</td>
<td>Dim mode VCO pin discharge current</td>
<td>—</td>
<td>16.0</td>
<td>—</td>
<td>( \mu \text{A} )</td>
<td></td>
</tr>
<tr>
<td>( I_{VCOPK} )</td>
<td>Amplitude control VCO pin charging current</td>
<td>—</td>
<td>60.0</td>
<td>—</td>
<td>( \mu \text{A} )</td>
<td>( V_{CPH} &lt; 5V, \ V_{CS} &gt; V_{IPH} )</td>
</tr>
<tr>
<td>( t_{DTLO} ) (IR21592)</td>
<td>LO output deadtime</td>
<td>—</td>
<td>1.8</td>
<td>—</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>( t_{DTHO} ) (IR21592)</td>
<td>HO output deadtime</td>
<td>—</td>
<td>1.8</td>
<td>—</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>( t_{DTLO} ) (IR21593)</td>
<td>LO output deadtime</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>( t_{DTHO} ) (IR21593)</td>
<td>HO output deadtime</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
</tbody>
</table>

### Gate Driver Output Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( VOH )</td>
<td>High-level output voltage</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>( V_{BIAS} - V_o )</td>
</tr>
<tr>
<td>( VOL )</td>
<td>Low-level output voltage</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( tr )</td>
<td>Turn-on rise time</td>
<td>—</td>
<td>—</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( tf )</td>
<td>Turn-off fall time</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics (cont.)

$V_{CC} = V_{BS} = V_{BIAS} = 14\, V \pm 0.25\, V$, $V_{CS} = 0.5\, V$, $V_{SD} = 0.0\, V$, $R_{FMIN} = 40\, k\Omega$, $C_{VCO} = 10\, nF$, $V_{DIM} = 0.0\, V$, $R_{MAX} = 33\, k\Omega$, $R_{MIN} = 56\, k\Omega$, $V_{TPH} = 0.0\, V$, $C_{LO,HO} = 1000\, pF$, $T_A = 25^\circ C$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CPH}$</td>
<td>CPH pin charging current</td>
<td>—</td>
<td>1.3</td>
<td>—</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{CPHIGN}$</td>
<td>CPH pin ignition mode threshold voltage</td>
<td>—</td>
<td>5.0</td>
<td>—</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{CPHCLMP}$</td>
<td>CPH pin clamp voltage</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IPH}$</td>
<td>IPH pin DC source current</td>
<td>—</td>
<td>25.0</td>
<td>—</td>
<td>$\mu A$</td>
<td>$I_{IPH} = 1/R_{FMIN}$</td>
</tr>
<tr>
<td>$V_{CSTH}$</td>
<td>Peak preheat current regulation threshold</td>
<td>—</td>
<td>0.7</td>
<td>—</td>
<td>$V$</td>
<td>$V_{CSTH} = (I_{IPH}) \times (R_{IPH})$</td>
</tr>
<tr>
<td>$V_{CPHFLT}$</td>
<td>CPH pin voltage during UVLO or fault</td>
<td>—</td>
<td>0.0</td>
<td>—</td>
<td>$V$</td>
<td>$SD = 5, V$, or $CS = 2, V$, or $T_j &gt; TSD$</td>
</tr>
</tbody>
</table>

#### Ignition Detection

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IPHIGN+}$</td>
<td>IPH source current (Vcs rising)</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>$\mu A$</td>
<td>$V_{CPH} &gt; 5.1, V$, $V_{CS} &lt; V_{IPH}$</td>
</tr>
<tr>
<td>$I_{IPHIGN-}$</td>
<td>IPH source current (Vcs falling)</td>
<td>—</td>
<td>27.5</td>
<td>—</td>
<td>$\mu A$</td>
<td>$V_{CPH} &gt; 5.1, V$, $V_{CS} &gt; V_{IPH}$</td>
</tr>
</tbody>
</table>

#### Protection Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SDTH+}$</td>
<td>Rising shutdown pin threshold voltage</td>
<td>—</td>
<td>2.0</td>
<td>—</td>
<td>$V$</td>
<td>$V_{CPH} &lt; 5, V$</td>
</tr>
<tr>
<td>$V_{CSTH}$</td>
<td>Peak over current threshold</td>
<td>—</td>
<td>1.6</td>
<td>—</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{VDCTH+}$</td>
<td>Rising VDC pin threshold voltage</td>
<td>—</td>
<td>5.1</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SDHY}$</td>
<td>SD threshold hysteresian</td>
<td>—</td>
<td>150</td>
<td>—</td>
<td>$mV$</td>
<td></td>
</tr>
<tr>
<td>$V_{VDCHY}$</td>
<td>VDC threshold hysteresian</td>
<td>—</td>
<td>2.1</td>
<td>—</td>
<td>$V$</td>
<td>$ISD = 100, mA$</td>
</tr>
<tr>
<td>$V_{SDCLMP}$</td>
<td>SD pin clamp voltage</td>
<td>—</td>
<td>7.6</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CSTH}$</td>
<td>Peak over-current latch threshold voltage</td>
<td>—</td>
<td>1.6</td>
<td>—</td>
<td></td>
<td>$V_{CPH} &gt; 5.1, V$</td>
</tr>
<tr>
<td>$T_{SD}$</td>
<td>Thermal shutdown junction temperature</td>
<td>—</td>
<td>165</td>
<td>—</td>
<td>$^\circ C$</td>
<td></td>
</tr>
</tbody>
</table>

#### Phase Control

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CSTHZX}$</td>
<td>Zero-crossing threshold voltage</td>
<td>—</td>
<td>0.0</td>
<td>—</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$R_{FB}$</td>
<td>Phase control FB resistor (Internal)</td>
<td>—</td>
<td>5.7</td>
<td>—</td>
<td>$k\Omega$</td>
<td></td>
</tr>
<tr>
<td>$T_{BLANK}$</td>
<td>Zero-crossing internal blank time</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>$ns$</td>
<td></td>
</tr>
</tbody>
</table>

#### Dimming Interface

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DIMOFF}$</td>
<td>DIM pin offset voltage</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DIM}$</td>
<td>DIM pin input voltage range</td>
<td></td>
<td>0.0</td>
<td>5.0</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{MINMIN}$</td>
<td>DIM minimum reference voltage (MIN pin)</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>$V$</td>
<td>$V_{DIM} = 5, V$</td>
</tr>
<tr>
<td>$V_{MINMAX}$</td>
<td>DIM maximum reference voltage (MIN pin)</td>
<td>—</td>
<td>3.0</td>
<td>—</td>
<td>$V$</td>
<td>$V_{DIM} = 0, V$</td>
</tr>
<tr>
<td>$V_{DIMTH}$</td>
<td>DIM mode VCO Threshold (IR21592)</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DIMTH}$</td>
<td>DIM mode VCO Threshold (IR21593)</td>
<td>—</td>
<td>1.1</td>
<td>—</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Minimum Frequency Setting

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FMIN}$</td>
<td>FMIN pin voltage during normal operation</td>
<td>—</td>
<td>5.1</td>
<td>—</td>
<td>$V$</td>
<td>$SD = 5, V$, or $CS = 2, V$, or $T_j &gt; TSD$</td>
</tr>
<tr>
<td>$V_{FMINFLT}$</td>
<td>FMIN pin voltage during fault mode</td>
<td>—</td>
<td>0.0</td>
<td>—</td>
<td>$V$</td>
<td></td>
</tr>
</tbody>
</table>
Lead Assignments & Definitions

<table>
<thead>
<tr>
<th>Pin Assignments</th>
<th>Pin #</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDC</td>
<td>1</td>
<td>VDC</td>
<td>Line input voltage detection</td>
</tr>
<tr>
<td>VCO</td>
<td>2</td>
<td>VCO</td>
<td>Voltage controlled oscillator input</td>
</tr>
<tr>
<td>CPH</td>
<td>3</td>
<td>CPH</td>
<td>Preheat timing input</td>
</tr>
<tr>
<td>DIM</td>
<td>4</td>
<td>DIM</td>
<td>0.5 to 5VDC dimming control input</td>
</tr>
<tr>
<td>MAX</td>
<td>5</td>
<td>MAX</td>
<td>Maximum lamp power setting</td>
</tr>
<tr>
<td>MIN</td>
<td>6</td>
<td>MIN</td>
<td>Minimum lamp power setting</td>
</tr>
<tr>
<td>FMIN</td>
<td>7</td>
<td>FMIN</td>
<td>Minimum frequency setting</td>
</tr>
<tr>
<td>IPH</td>
<td>8</td>
<td>IPH</td>
<td>Peak preheat current reference</td>
</tr>
<tr>
<td>SD</td>
<td>9</td>
<td>SD</td>
<td>Shutdown input</td>
</tr>
<tr>
<td>CS</td>
<td>10</td>
<td>CS</td>
<td>Current sensing input</td>
</tr>
<tr>
<td>LO</td>
<td>11</td>
<td>LO</td>
<td>Low-side gate driver output</td>
</tr>
<tr>
<td>COM</td>
<td>12</td>
<td>COM</td>
<td>IC power &amp; signal ground</td>
</tr>
<tr>
<td>VCC</td>
<td>13</td>
<td>VCC</td>
<td>Logic &amp; low-side gate driver supply</td>
</tr>
<tr>
<td>VS</td>
<td>14</td>
<td>VS</td>
<td>High-side gate driver floating supply</td>
</tr>
<tr>
<td>VB</td>
<td>15</td>
<td>VB</td>
<td>High voltage floating return</td>
</tr>
<tr>
<td>HO</td>
<td>16</td>
<td>HO</td>
<td>High-side gate driver output</td>
</tr>
</tbody>
</table>
State Diagram

Power Turned On

UVLO Mode
1/2-Bridge Off
IQCC=200mA
CPH=0V
Oscillator Off

SD > 2.0V
(Lamp Removal)
or
VCC < 10.9V
(Power Turned Off)

VCC < 10.9V
(VCC Fault or Power Down)
or
VDC < 3.0V
(dc Bus/ac Line Fault or Power Down)
or
SD > 2.0V
(Lamp Fault or Lamp Removal)

FAULT Mode
Fault Latch Set
1/2-Bridge Off
IQCC=240mA
CPH=0V
VCC=15.6V
Oscillator Off

TJ > 165°C
(Over-Temperature)

CS > V_CSTH (1.6V)
(Failure to Strike Lamp
or Hard Switching)
or
TJ > 165°C
(Over-Temperature)

PREHEAT Mode
1/2-Bridge Oscillator On
V_CSPK + V_IPH (Peak
Current Control)
CPH Charging@I_PPH + 1µA
DIM=Open Circuit
Over-Current Disabled

CPH > 5.1V
(End of PREHEAT Mode)

IGNITION Mode
f_PH ramps to f_MIN
CPH Charging@I_PPH + 1µA
DIM=Open Circuit
Over-Current Enabled

CS > V_CSTH (1.6V)
(Over-Current or Hard Switching)
or
TJ > 165°C
(Over-Temperature)

DIM Mode
Phase=Phase_REF
DIM=CPH
Over-Current Enabled

VCC > 12.5V
(UV+)
and
VDC > 5.1V
(Bus OK)
and
SD < 1.7V
(Lamp OK)
and
TJ < 165°C
(Tj_max)

DIM+Open Circuit
Over-Current Disabled

TJ > 165°C
(Over-Temperature)

CS > V_CSTH (1.6V)
(Over-Current or Hard Switching)
or
TJ > 165°C
(Over-Temperature)

V_CSPK > V_IPH (enable ignition detection)
then
V_CS < V_PIN (ignition detected)
Timing Diagram
Non-strike fault condition with lamp exchange
External Components Selection Procedure

(Note: Please refer to “Typical Connection” diagram, page 1)

**BEGIN**

- **Calculate** \( R_{\text{pull-up}} \)
  \[
  R_{\text{pull-up}} = \frac{V_{\text{AC turn-on}}}{I_{\text{QCVV}}}
  \]

- **Calculate** \( R_{\text{VDC}} \)
  \[
  R_{\text{DC}} = \frac{\frac{5.1}{V_{\text{AC turn-on}}}}{1 - \frac{5.1}{V_{\text{AC turn-on}}}}
  \]

- **Select** \( R_{\text{FMIN}} \)
  Use Graph 5 or Graph 6

- **Select & Calculate** \( R_{\text{IPH}} \)
  Use Graph 8 to find \( I_{\text{IPH}} \), then calculate \( R_{\text{IPH}} \): 
  \[
  R_{\text{IPH}} = \frac{I_{\text{IPH} \cdot R_{\text{CS}}}}{I_{\text{IPH}}}
  \]

- **Calculate** \( C_{\text{CPH}} \)
  \[
  C_{\text{CPH}} = (2.6 e^{-7}) I_{\text{IPH}}
  \]

- **Calculate** \( R_{\text{MIN}} \)
  Find \( I_{\text{MIN}} \) (Graph 7)
  Calculate \( \phi_{\text{MIN}} \) (Equations 8 & 9)
  Find \( V_{\text{MIN}} \) (Graph 9)
  \[
  R_{\text{MIN}} = \frac{V_{\text{MIN}}}{I_{\text{MIN}}}
  \]

- **Calculate** \( R_{\text{MAX}} \)
  Use Equation 15

**Set** \( R_{\text{CS}} \) and \( R_{\text{VDC}} \) such that the voltage on pin VDC will exceed 5.1 volts at the desired line turn-on voltage.

The minimum operating frequency must be lower than \( f_{\text{IGN}} \) of \( r_{\text{IGN}} \) (whichever is lower). \( R_{\text{MIN}} \) also programs \( I_{\text{MIN}} \) and \( I_{\text{MIN}} \), so \( R_{\text{MIN}} \) must be set first.

\( R_{\text{CS}} \) sets the maximum ignition current which corresponds to the maximum ignition voltage across the lamp.

The voltage at pin IPH is the reference for amplitude current control during preheat mode. \( R_{\text{MIN}} \) must be set after \( R_{\text{MIN}} \).

During preheat, an internal 1.3\( \mu \)A current source at pin CPH charges external capacitor CCPH. Preheat mode ends when VCPH exceeds 5.1 volts.

\( R_{\text{MIN}} \) sets the lower phase boundary corresponding to minimum lamp power when \( V_{\text{DIM}} = 0 \) volts. \( R_{\text{MIN}} \) must be set after \( R_{\text{MIN}} \).

\( R_{\text{MAX}} \) sets the upper phase boundary corresponding to maximum lamp power when \( V_{\text{DIM}} = 5 \) volts. \( R_{\text{MAX}} \) must be set after \( R_{\text{MAX}} \) and \( R_{\text{MIN}} \).
Characteristic Curves

Graph 1. Frequency vs $V_{VCO}$ (IR21592)

Graph 2. Frequency vs $V_{VCO}$ (IR21593)

Graph 3. Frequency vs $R_{FMN}$ (IR21592)

Graph 4. Frequency vs $R_{FMN}$ (IR21593)
Graph 5. Frequency vs R_{FMIN} (IR21592)

Graph 6. Frequency vs R_{FMIN} (IR21593)

Graph 7. I_{MIN} vs R_{FMIN} (IR21592/IR21593)

Graph 8. I_{PH} vs R_{FMIN} (IR21592/IR21593)
Graph 9. $\phi$ VS $V_{MIN}$ (IR21592/IR21593)  

Graph 10. $R_{MIN}$ VS $V_{MIN}$  

Graph 11. $I_{CPH}$ VS Temperature (IR21592/IR21593)  

Graph 12. $I_{MIN}$ VS Temperature (IR21592/IR21593)
Graph 13. $I_{PH}$ vs Temperature (IR21592/IR21593)

Graph 14. $V_{FMIN}$ vs Temperature (IR21592/IR21593)

Graph 15. Frequency vs Temperature $V_{VCO}=0V$ (IR21592/IR21593)

Graph 16. Frequency vs Temperature $V_{VCO}=2V$ (IR21592/IR21593)
Graph 17. Dead Time vs Temperature
(IR21592/IR21593)
Functional Description

Phase Control

To understand phase control, a simplified model for the ballast output stage is used (Figure 1). The lamp and filaments are replaced with resistors, with the lamp inserted between the filament resistors (R1, R2, R3 and R4).

During preheat and ignition (Figure 2), the circuit is a high-Q series LC with a strong input current to input voltage phase inversion from +90 to -90 degrees at the resonance frequency. For operating frequencies slightly above resonance and higher, the phase is fixed at -90 degrees for the duration of preheat and ignition. During dimming, the circuit is an L in series with a parallel R and C, with a weak phase inversion at high lamp power and a strong phase inversion at low lamp power.

In the time domain (Figure 3), the input current is shifted -90 degrees from the input half-bridge voltage during preheat and ignition, and somewhere between 0 and -90 degrees after ignition during running. Zero phase-shift corresponds to maximum power.

When the phase is calculated and plotted versus lamp power (Figure 4), the result is a linear dimming curve, even down to ultra-low light levels where the resistance of the lamp can change by orders of magnitude.
Under-voltage Lock-Out (UVLO)

The IR21592/IR21593 undervoltage lock-out is designed to maintain an ultra low quiescent current of less than 200μA, while guaranteeing the IC is fully functional before the high and low side output drivers are activated. Figure 5 shows an efficient supply voltage using the start-up current of the IR21592/IR21593 together with a charge pump from the ballast output stage (R1, C1, C2, D1 and D2).

During the discharge cycle, the rectified current from the charge pump charges the capacitor above the minimum operating voltage of the device and the charge pump and internal 15.6V zener clamp of the IC take over as the supply voltage. The start-up capacitor and snubber capacitor must be selected such that worst case IC conditions are satisfied. A bootstrap diode (D3) and supply capacitor (C3) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During UVLO, the high and low side driver outputs are low, pin VCO is pulled-up internally to 5V resetting the starting frequency to the maximum, and pin CPH is short-circuited internally to COM resetting the preheat time.

The start-up capacitor (C1) is charged by current through resistor (R1) minus the start-up current drawn by the IC. This resistor is typically chosen to provide 2X the maximum start-up current at low line to guarantee start-up under the worst case condition. Once the capacitor voltage reaches the start-up threshold, and, the voltage on pin VDC is above 5.1V (see Brown-out Protection), the IC turns on and HO and LO begin to oscillate. The capacitor begins to discharge due to the increase in IC operating current (Figure 6).
Brown-out Protection

In addition to the voltage on VCC being above the start-up threshold, pin VDC must also be above 5.1V for HO and LO to begin oscillating. A voltage divider (R3, RVDC) from the rectified AC line connected to pin VDC measures the rectified AC line input voltage to the ballast and programs the turn-on and turn-off line voltages. A filter capacitor (CVDC) is also connected to pin VDC that must be chosen such that the ripple is low enough and the lower turn-off threshold of 3V is not crossed during normal line conditions. This detection is necessary due to the possibility of the lamp extinguishing during low-line conditions before the IC is properly reset. Should a brown-out occur, the DC bus can drop to a level below the minimum required for the tank circuit to maintain the necessary lamp voltage. This detection will insure a clean turn-off before the DC bus drops too low and properly resets the IC to the preheat mode when the line returns.

Preheat (PH)

The IR21592/IR21593 enters preheat mode when VCC exceeds the UVLO+ threshold and VDC exceeds 5.1V. HO and LO begin to oscillate at the maximum operating frequency with 50% duty cycle and at the internally set dead-time of 2us. Pin CPH is disconnected from COM and an internal 1uA current source (Figure 7) charges the external timing capacitor on CPH linearly.

An internal 1uA current source slowly discharges the external capacitor on pin VCO and the voltage on pin VCO begins to decrease. This decreases the frequency, which, for operating frequencies above resonance, increases the load current. When the peak voltage measured on pin CS, produced by a portion of the load current flowing through an external sense resistor (RCS), exceeds the voltage level on pin IPH, a 60uA internal current source is connected to pin VCO and the capacitor charges (Figure 8). This forces the frequency to increase and the load current to decrease. When the voltage on pin CS decreases below IPH, the 60uA current source is disconnected and the frequency decreases again.
This feedback keeps the peak preheat current regulated to the user-programmable setting on pin IPH for the duration of the preheat time. An internal current source connected to an external resistor on pin IPH sets a voltage reference for the peak preheat current. The preheat time continues until the voltage on pin CPH exceeds 5V.

**Ignition (IGN)**

The IR21592/IR21593 enters ignition mode when the voltage on pin CPH exceeds 5V. The peak current regulation reference voltage is disconnected from the user-programmable setting on pin IPH and is connected to a higher internal threshold of 1.6V (Figure 9).

The ignition ramp is then initiated as the capacitor on pin VCO discharges linearly through an internal 1uA current source. The frequency decreases linearly towards the resonance frequency of the high-Q ballast output stage, causing the lamp voltage and load current to increase (Figure 10). The frequency continues to decrease until the lamp ignites or the current limit of the IR21592/IR21593 is reached. If the current limit is reached, the IR21592/IR21593 enters FAULT mode. The 1.6V threshold together with the external current sensing resistor on pin CS determine the maximum allowable peak ignition current (and therefore peak ignition voltage) of the ballast output stage. The peak ignition current must not exceed the maximum allowable current ratings of the output stage MOSFETs or IGBTs, and, the resonant inductor must not saturate at any time.

To prevent a “flash” across the lamp during ignition at low dim settings, an ignition detection...
circuit measures the voltage at the CS pin and compares it against the voltage at the IPH pin. During the rising ignition ramp, the voltage at the IPH pin is increased to 20% above its value during preheat mode. When the voltage on the CS pin exceeds this voltage, the voltage on the IPH pin is decreased to 10% and the ignition detection circuit is then active (See Figure 10). When the lamp ignites, the voltage on the CS pin will then fall below the voltage on the IPH pin and the IC enters DIM Mode and the phase control loop is closed. In order for the ignition detection circuit to function properly and for the IC to enter DIM mode, the voltage on the CS pin must first rise above VIPH + 20% during the ignition ramp to activate the circuit, and then decrease below VIPH + 10% when the lamp ignites.

**Ignition-to-Dim (IGN-to-DIM)**

When the IR21592/IR21593 enters dim mode, the phase control loop is closed and the phase of the load current is regulated against the user control input on pin DIM. To control the rate at which the dim setting changes from maximum brightness to the user setting (IGN-TO-DIM time, Figure 11), pin DIM is connected internally to pin CPH when the IR21592/IR21593 enters DIM mode. The resistor on pin DIM (RDIM) discharges the capacitor on pin CPH down to the user dim setting. The resistor can be selected for a fast time constant to minimize the amount of flash visible over the lamp just after ignition, or, a long time constant such that the brightness ramps down smoothly to the user setting. Should the ignition-to-dim time be too fast, however, the loop can respond faster than the ionization constant of the lamp (milliseconds) causing the VCO to over-shoot. This can result in a frequency that is higher than the minimum brightness frequency and can extinguish the lamp. The capacitor on pin CPH serves multiple functions by setting the preheat time, the travel rate just after ignition (together with resistor RDIM), and, serving as a filter capacitor on pin
Once lock is achieved, the phase detector (PDET) outputs short pulses to an open-drain PMOS that charges the VCO capacitor through an internal resistor (RFB) each time an error pulse occurs (Figure 13). This action "nudges" the integrator at the input of the VCO to keep the phase of the output stage current exactly locked in phase with the reference.

DIM during dimming to increase high-frequency noise immunity and minimize component count.

**Dimming (DIM)**

To regulate lamp power, the error between the reference phase and the phase of the output stage current forces the VCO to steer the frequency in the proper direction, as determined by the transfer function of the output stage, such that the error is forced to zero. An internal 15uA current source is connected to pin VCO during dimming mode (Figure 12) to discharge the VCO capacitor and decrease the frequency towards lock.

The IR21592/IR21593 includes a dimming interface for analog lamp power control. The DIM pin input requires a voltage in the range of 0.5 to 5VDC, with 5V corresponding to minimum phase shift (maximum lamp power). The output of the dim interface is the voltage on pin MIN, which is compared with the internal timing capacitor (CT) voltage to produce a frequency-independent digital reference phase (Figure 14).
The charging time of CT from 1V to 5.1V determines the on-time of output gate drivers HO and LO and corresponds to -180 degrees of possible phase shift in load current (minus deadtime). For the 0 to -90 degree dim range, the voltage on pin MIN is bounded between 1V and 3V using pins MIN and MAX. An external resistor on pin MAX programs the minimum phase shift reference (maximum lamp power) corresponding to 5V on pin DIM, and an external resistor on pin MIN sets the maximum phase shift (minimum lamp power) corresponding to 0.5V on pin DIM.

**Current Sensing**

During dimming, the current sensing circuitry (Figure 15) detects over-current which can occur during hard-switching (see Fault section), and zero-crossing to measure the phase of the total load current. To reject any switching noise which can occur at the turn-on of the low-side MOSFET or IGBT, a digital current sense blanking circuit blanks out the signal from the zero-crossing detection comparator for 400ns after LO goes 'high' (Figure 16).

The internal blank time reduces the dimming range slightly (Figure 16) when operating at minimum phase shift (maximum lamp power). The external programming resistor on pin MAX must be selected such that the minimum phase shift is set a safe margin away from the blank time. A series resistor (R1) is required to limit the amount of current flowing out of pin CS when the voltage across RCS goes below -0.7V. A filter capacitor at pin CS may be required due to other possible asynchronous noise sources present in the ballast system.
The internal blank time reduces the dimming range slightly (Figure 16) when operating at minimum phase shift (maximum lamp power). The external programming resistor on pin MAX must be selected such that the minimum phase shift is set a safe margin away from the blank time. A series resistor (R1) is required to limit the amount of current flowing out of pin CS when the voltage across RCS goes below -0.7V. A filter capacitor at pin CS may be required due to other possible asynchronous noise sources present in the ballast system.

Fault Mode (FAULT)

During dimming, the peak current regulation circuit active during preheat and ignition is disabled. Should non-zero voltage switching at the output of the half-bridge occur (Figure 17), high current spikes will result. A lamp filament failure, lamp end-of-life, lamp removal, or a deadtime shorter than what is required for commutation, can all cause hard-switching.
Should the peak voltage on pin CS exceed 1.6V at any time during dimming, the IR21592/IR21593 enters FAULT mode and the high and low-side driver outputs, HO and LO, are both turned off. Cycling the supply voltage on VCC below or the voltage on pin SD will reset the IR21592/IR21593 to preheat (PH) mode (see STATE DIAGRAM).

**Ballast Design**

**Lamp Requirements**

Before selecting component values for the ballast output stage and the programmable inputs of the IR21592/IR21593, the following lamp requirements must first be defined:

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ph}$</td>
<td>Filament pre-heat current</td>
<td>Arms</td>
</tr>
<tr>
<td>$t_{ph}$</td>
<td>Filament pre-heat time</td>
<td>s</td>
</tr>
<tr>
<td>$V_{ph_{max}}$</td>
<td>Maximum lamp pre-heat voltage</td>
<td>Vpp</td>
</tr>
<tr>
<td>$V_{ign}$</td>
<td>Lamp ignition voltage</td>
<td>Vpp</td>
</tr>
<tr>
<td>$P_{100%}$</td>
<td>Lamp power at 100% brightness</td>
<td>W</td>
</tr>
<tr>
<td>$V_{100%}$</td>
<td>Lamp voltage at 100% brightness</td>
<td>Vpp</td>
</tr>
<tr>
<td>$P_1%$</td>
<td>Lamp power at 1% brightness</td>
<td>W</td>
</tr>
<tr>
<td>$V_1%$</td>
<td>Lamp voltage at 1% brightness</td>
<td>Vpp</td>
</tr>
<tr>
<td>$I_{cath_{min}}$</td>
<td>Minimum cathode heating current</td>
<td>Arms</td>
</tr>
</tbody>
</table>

Table I, Typical lamp requirements

**Ballast Output Stage**

The components comprising the output stage are selected using a set of equations. Different ballast operating frequencies and their respective voltages and currents are calculated.

The inductor and capacitor values are obtained using equations (2) through (7). The results of these equations reveal the location of each operating frequency and the corresponding voltages and currents. For a given L, C, DC bus voltage, and pre-heat current, the resulting voltage over the lamp during pre-heat is given as:

$$V_{ph} = \left[ \left( \frac{2V_{DC}}{\pi} \right)^2 + \frac{8L}{C} I_{ph}^2 \right]^{\frac{1}{2}} - \frac{2V_{DC}}{\pi} \quad (2)$$

The resulting operating frequency during pre-heat is given as:

$$f_{ph} = \frac{\sqrt{2I_{ph}}}{\pi CV_{ph}} \quad [\text{Hz}] \quad (3)$$

The resulting operating frequency during ignition is given as:

$$f_{ign} = \frac{1}{2\pi} \sqrt{1 + \frac{4V_{DC}}{V_{ign} LC}} \quad [\text{Hz}] \quad (4)$$

The total load current during ignition is given as:

$$I_{ign} = f_{ign} CV_{ign} 2\pi \quad [\text{App}] \quad (5)$$
The operating frequency [Hz] at maximum lamp power is given as:

\[ f_{\text{max}} = \frac{1}{2\pi} \left[ \frac{1}{LC} - \frac{32p_{\text{min}}^2}{C\sqrt{V_{\text{min}}}} \right] - \frac{1}{E^2} \left( \frac{4V_{\text{DC}}}{V_{\text{dc}}} \right) \] (6)

The cathode heating current at minimum lamp power is given as:

\[ I_{\text{ Cath}_{\text{min}}} = \frac{V_{1\%} f_{\text{max}} \pi C}{\sqrt{2}} \] (7)

**Design Constraints**

The inductor and capacitor values should be iterated until the following design constraints have been fulfilled (Table II).

<table>
<thead>
<tr>
<th>Design Constraint</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{ph}} &lt; V_{\text{ph max}} )</td>
<td>Ignition during pre-heat</td>
</tr>
<tr>
<td>( f_{\text{ph}} - f_{\text{ign}} &gt; 5 \text{kHz} )</td>
<td>Production tolerances</td>
</tr>
<tr>
<td>( I_{\text{ign}} &lt; I_{\text{ign max}} )</td>
<td>Inductor saturation</td>
</tr>
<tr>
<td>( I_{\text{Cath}<em>{\text{min}}} \geq I</em>{\text{Cath}_{\text{min}}} )</td>
<td>Lamp extinguishing during dimming</td>
</tr>
</tbody>
</table>

Table II, Ballast design constraints

**IR21592/IR21593 Programmable Inputs**

In order to program the MIN and MAX settings of the dimming interface, the phase of the output stage current at minimum and maximum lamp power must be calculated. This is obtained using the following equations:

\[ R_{\text{MIN}} = \frac{R_{\text{FMIN}}}{4} \left( 1 - \frac{\phi_{1\%}}{45} \right) \] (14)

\[ R_{\text{MAX}} = \frac{0.86 \cdot R_{\text{FMIN}} \cdot R_{\text{MIN}}}{4 \cdot R_{\text{MIN}} - R_{\text{FMIN}} \left( 1 - \frac{\phi_{100\%}}{45} \right)} \] (15)
This ballast design procedure has been summarized into the following 3 steps:

1. Define Lamp Requirements
2. Iterate L and C to fulfill constraints
3. Calculate IR21592/IR21593 Programmable Inputs

Figure 19, Simplified Ballast Design Procedure

Case outline

16 Lead PDIP

NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDC OUTLINE MS-D022AA.
5. MEASURED WITH THE LEADS CONstrained TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.25 (.010).