

MC14553B

3-Digit BCD Counter

The MC14553B 3-digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|--------------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in} | Input Current (DC or Transient) per Pin | ± 10 | mA |
| I_{out} | Output Current (DC or Transient) per Pin | +20 | mA |
| P_D | Power Dissipation, per Package (Note 2.) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}\text{C}$ |

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

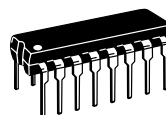
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



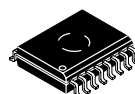
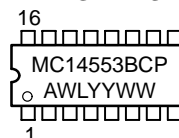
ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAMS



PDIP-16
P SUFFIX
CASE 648



SOIC-16
DW SUFFIX
CASE 751G



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
|------------|---------|----------|
| MC14553BCP | PDIP-16 | 25/Rail |
| MC14553BDW | SOIC-16 | 47/Rail |

MC14553B

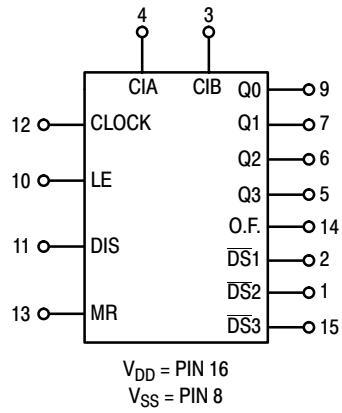


Figure 1. Block Diagram

TRUTH TABLE

| Inputs | | | | Outputs |
|--------------|-------|---------|----|-----------------------|
| Master Reset | Clock | Disable | LE | |
| 0 | | 0 | 0 | No Change |
| 0 | | 0 | 0 | Advance |
| 0 | X | 1 | X | No Change |
| 0 | 1 | | 0 | Advance |
| 0 | 1 | | 0 | No Change |
| 0 | 0 | X | X | No Change |
| 0 | X | X | | Latched |
| 0 | X | X | 1 | Latched |
| 1 | X | X | 0 | Q0 = Q1 = Q2 = Q3 = 0 |

X = Don't Care

MC14553B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit | | |
|---|--|---|-------------------------------------|-----------|-------|------------------|-----------|-------|-----------|-----------|------|------|
| | | | Min | Max | Min | Typ (Note 3.) | Max | Min | Max | | | |
| Output Voltage $V_{in} = V_{DD}$ or 0 | "0" Level V_{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | | |
| | $V_{in} = 0$ or V_{DD} | "1" Level V_{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc | |
| | | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | | |
| | | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | | |
| Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) | "0" Level V_{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | | |
| | $V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc) | "1" Level V_{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc | |
| | | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | | |
| | | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | | |
| Output Drive Current ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) | Source — Pin 3 I_{OH} | 5.0 | -0.25 | — | -0.2 | -0.36 | — | -0.14 | — | mAdc | | |
| | | 10 | -0.62 | — | -0.5 | -0.9 | — | -0.35 | — | | | |
| | | 15 | -1.8 | — | -1.5 | -3.5 | — | -1.1 | — | | | |
| | | 5.0 | -0.64 | — | -0.51 | -0.88 | — | -0.36 | — | | mAdc | |
| | | 10 | -1.6 | — | -1.3 | -2.25 | — | -0.9 | — | | | |
| | | 15 | -4.2 | — | -3.4 | -8.8 | — | -2.4 | — | | | |
| | $V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) | Sink — Pin 3 I_{OL} | 5.0 | 0.5 | — | 0.4 | 0.88 | — | 0.28 | — | mAdc | |
| | | | 10 | 1.1 | — | 0.9 | 2.25 | — | 0.65 | — | | |
| | | | 15 | 1.8 | — | 1.5 | 8.8 | — | 1.20 | — | | |
| | | $V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc) | Sink — Other Outputs I_{OL} | 5.0 | 3.0 | — | 2.5 | 4.0 | — | 1.6 | — | mAdc |
| | | | | 10 | 6.0 | — | 5.0 | 8.0 | — | 3.5 | — | |
| | | | | 15 | 18 | — | 15 | 20 | — | 10 | — | |
| Input Current | I_{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μ Adc | | |
| Input Capacitance ($V_{in} = 0$) | C_{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF | | |
| Quiescent Current (Per Package) $MR = V_{DD}$ | I_{DD} | 5.0 | — | 5.0 | — | 0.010 | 5.0 | — | 150 | μ Adc | | |
| | | 10 | — | 10 | — | 0.020 | 10 | — | 300 | | | |
| | | 15 | — | 20 | — | 0.030 | 20 | — | 600 | | | |
| Total Supply Current (Note 4., 5.) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching) | I_T | 5.0 | $I_T = (0.35 \mu A/kHz) f + I_{DD}$ | | | | | | | μ Adc | | |
| | | 10 | $I_T = (0.85 \mu A/kHz) f + I_{DD}$ | | | | | | | | | |
| | | 15 | $I_T = (1.50 \mu A/kHz) f + I_{DD}$ | | | | | | | | | |

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.004$.

MC14553B

SWITCHING CHARACTERISTICS (Note 6.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Figure | Symbol | V_{DD} | Min | Typ (Note 7.) | Max | Unit |
|---|--------|--------------------------|-----------------|--------------------|----------------------------|---------------------|---------------|
| Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | 2a | t_{TLH} , t_{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Clock to BCD Out | 2a | t_{PLH} , t_{PHL} | 5.0 10 15 | — — — | 900 500 200 | 1800 1000 400 | ns |
| Clock to Overflow | 2a | t_{PHL} | 5.0 10 15 | — — — | 600 400 200 | 1200 800 400 | ns |
| Reset to BCD Out | 2b | t_{PHL} | 5.0 10 15 | — — — | 900 500 300 | 1800 1000 600 | ns |
| Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time | 2b | t_{su} | 5.0 10 15 | 600 400 200 | 300 200 100 | — — — | ns |
| Removal Time Latch Enable to Clock | 2b | t_{rem} | 5.0 10 15 | - 80 - 10 0 | - 200 - 70 - 50 | — — — | ns |
| Clock Pulse Width | 2a | $t_{WH(cl)}$ | 5.0 10 15 | 550 200 150 | 275 100 75 | — — — | ns |
| Reset Pulse Width | 2b | $t_{WH(R)}$ | 5.0 10 15 | 1200 600 450 | 600 300 225 | — — — | ns |
| Reset Removal Time | — | t_{rem} | 5.0 10 15 | - 80 0 20 | - 180 - 50 - 30 | — — — | ns |
| Input Clock Frequency | 2a | f_{cl} | 5.0 10 15 | — — — | 1.5 5.0 7.0 | 0.9 2.5 3.5 | MHz |
| Input Clock Rise Time | 2b | t_{TLH} | 5.0 10 15 | No Limit | | | ns |
| Disable, MR, Latch Enable Rise and Fall Times | — | t_{TLH} , t_{THL} | 5.0 10 15 | — — — | — — — | 15 5.0 4.0 | μs |
| Scan Oscillator Frequency (C1 measured in μF) | 1 | f_{osc} | 5.0 10 15 | — — — | 1.5/C1 4.2/C1 7.0/C1 | — — — | Hz |

6. The formulas given are for the typical characteristics only at 25°C .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14553B

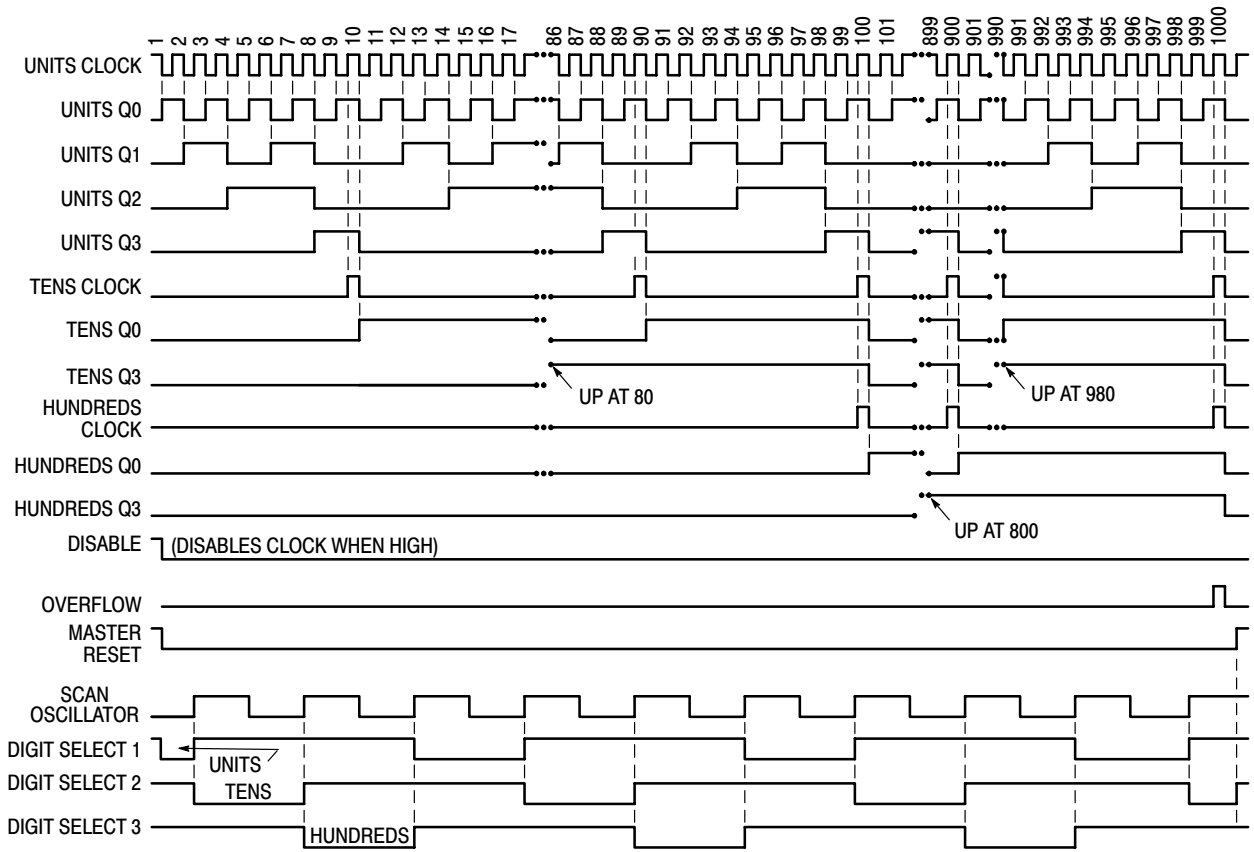


Figure 2. 3-Digit Counter Timing Diagram (Reference Figure 4)

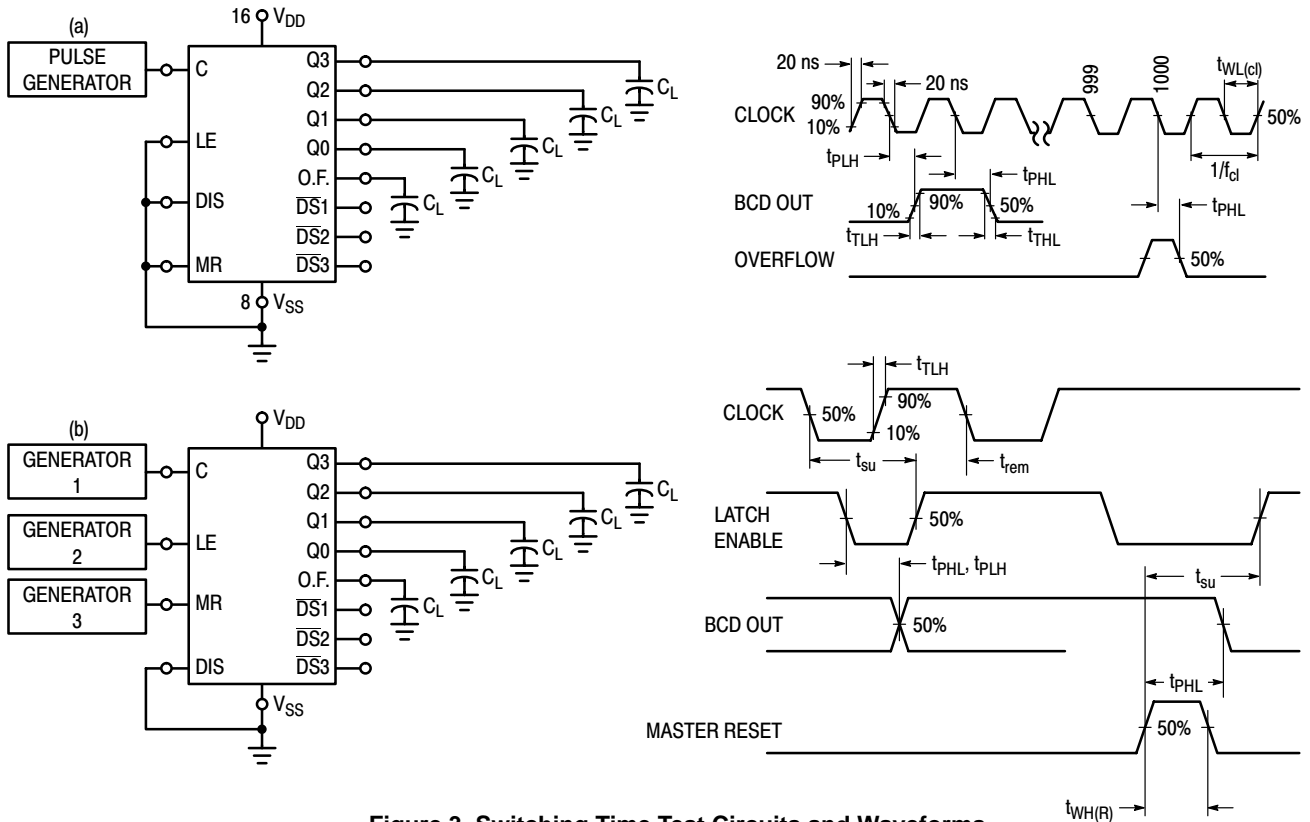


Figure 3. Switching Time Test Circuits and Waveforms

MC14553B

OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 4, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

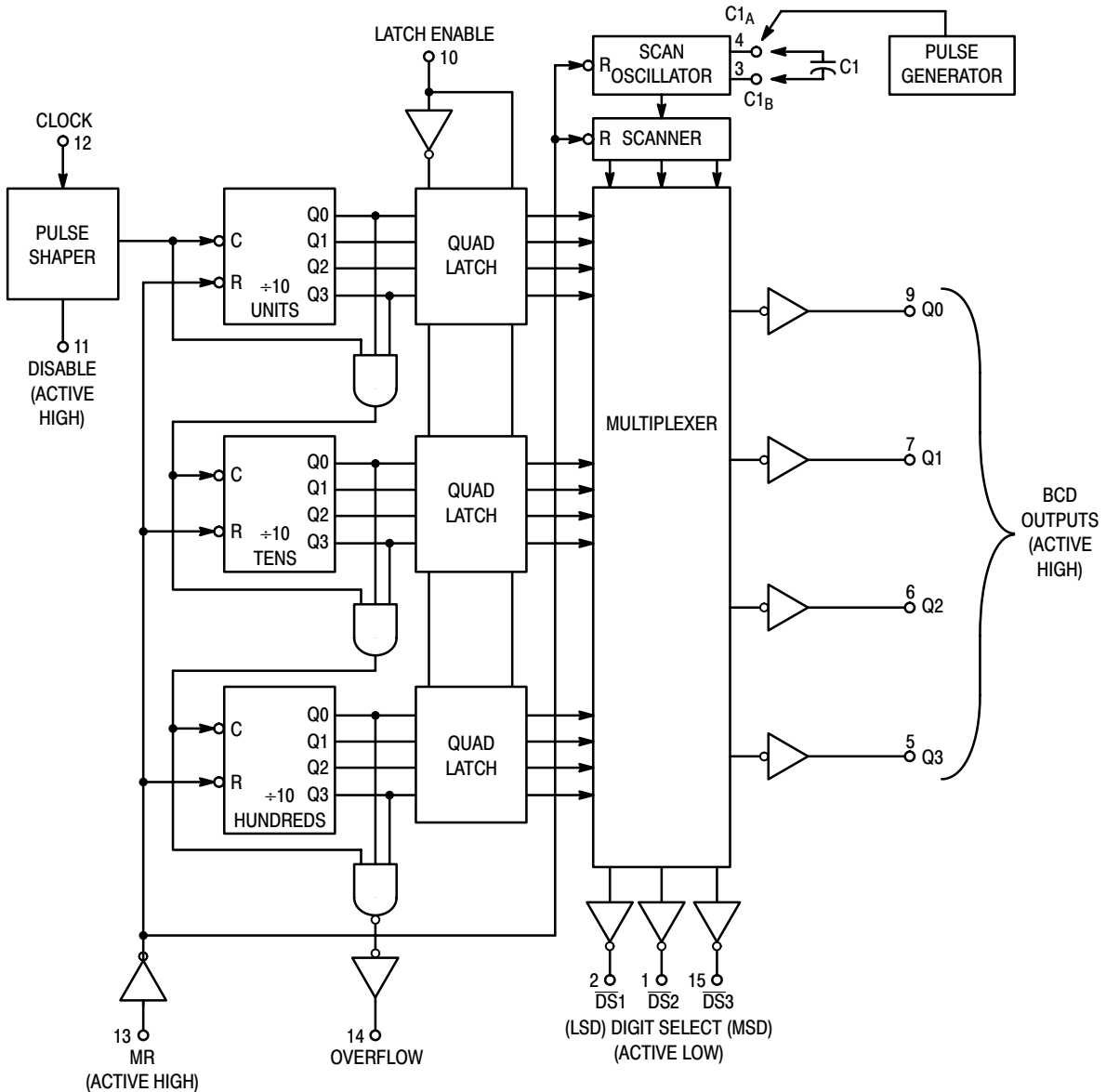


Figure 4. Expanded Block Diagram

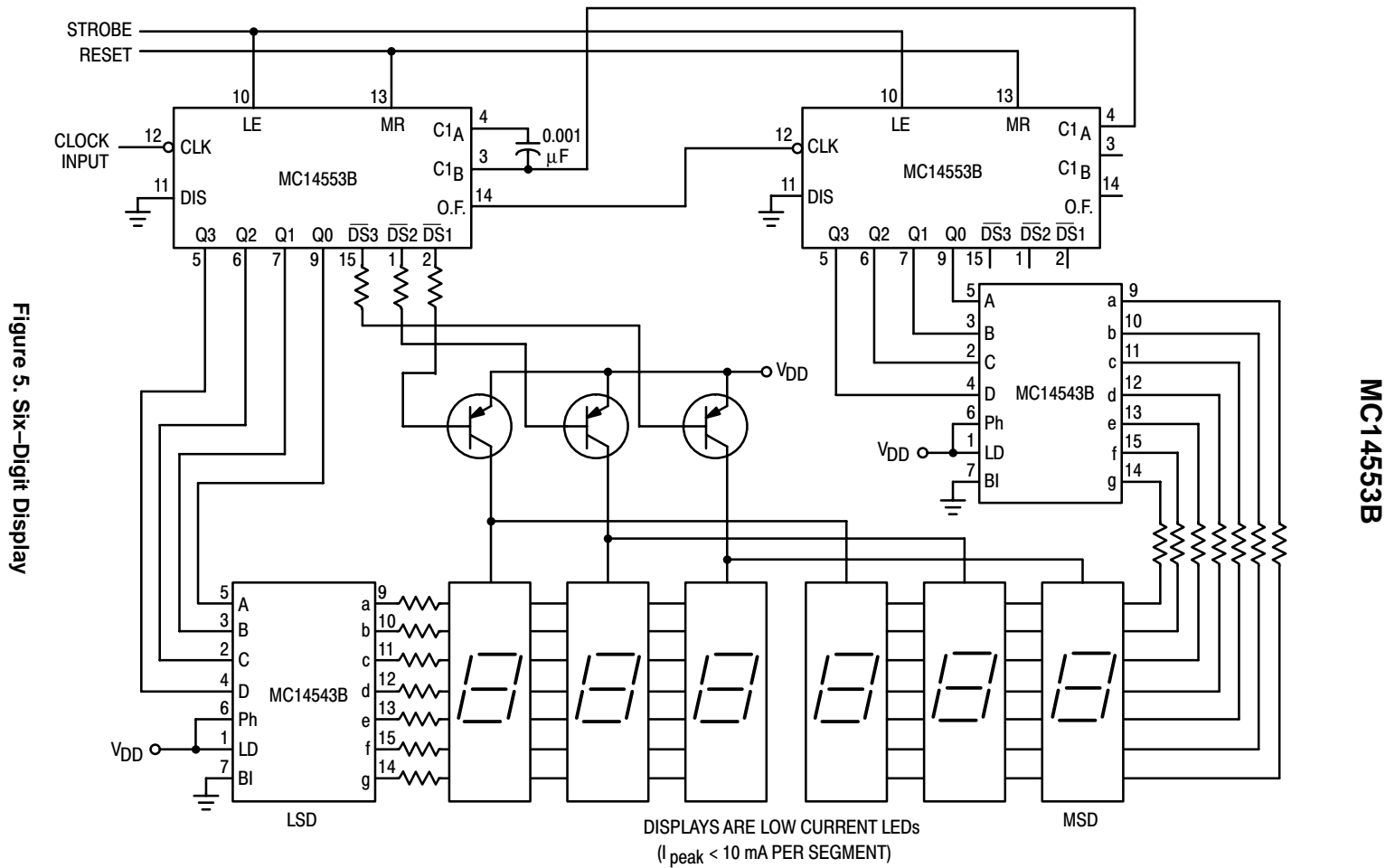


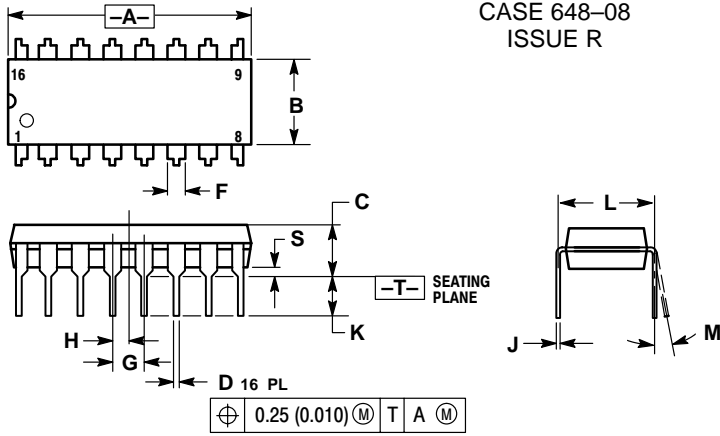
Figure 5. Six-Digit Display

MC14553B

MC14553B

PACKAGE DIMENSIONS

PDIP-16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE R



NOTES:

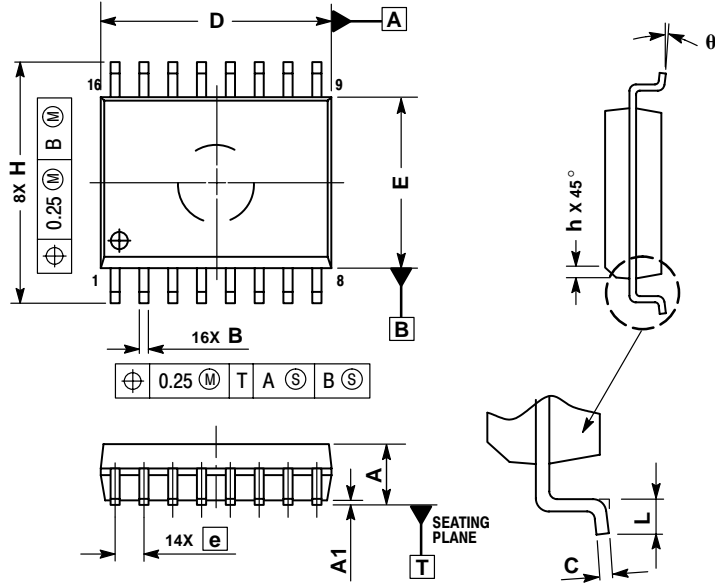
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

MC14553B

PACKAGE DIMENSIONS

SOIC-16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G-03
ISSUE B



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0 ° | 7 ° |

Notes

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.