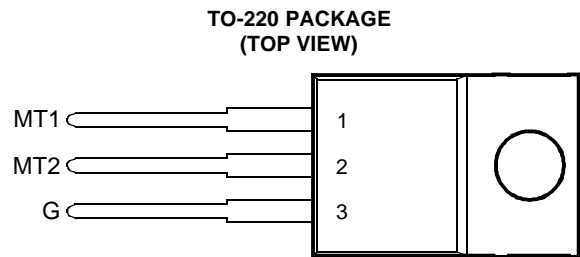


- Sensitive Gate Triacs
- 8 A RMS, 70 A Peak
- Glass Passivated Wafer
- 400 V to 800 V Off-State Voltage
- Max  $I_{GT}$  of 5 mA (Quadrant 1)



Pin 2 is in electrical contact with the mounting base.

MDC2ACA

### absolute maximum ratings over operating case temperature (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage (see Note 1)	TIC225D	$V_{DRM}$	400	V
	TIC225M		600	
	TIC225S		700	
	TIC225N		800	
Full-cycle RMS on-state current at (or below) 70°C case temperature (see Note 2)		$I_{T(RMS)}$	8	A
Peak on-state surge current full-sine-wave (see Note 3)		$I_{TSM}$	70	A
Peak on-state surge current half-sine-wave (see Note 4)		$I_{TSM}$	80	A
Peak gate current		$I_{GM}$	±1	A
Peak gate power dissipation at (or below) 85°C case temperature (pulse width ≤ 200 μs)		$P_{GM}$	2.2	W
Average gate power dissipation at (or below) 85°C case temperature (see Note 5)		$P_{G(AV)}$	0.9	W
Operating case temperature range		$T_C$	-40 to +110	°C
Storage temperature range		$T_{stg}$	-40 to +125	°C
Lead temperature 1.6 mm from case for 10 seconds		$T_L$	230	°C

- NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.  
 2. This value applies for 50-Hz full-sine-wave operation with resistive load. Above 70°C derate linearly to 110°C case temperature at the rate of 200 mA/°C.  
 3. This value applies for one 50-Hz full-sine-wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after the device has returned to original thermal equilibrium. During the surge, gate control may be lost.  
 4. This value applies for one 50-Hz half-sine-wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after the device has returned to original thermal equilibrium. During the surge, gate control may be lost.  
 5. This value applies for a maximum averaging time of 20 ms.

### electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{DRM}$ Repetitive peak off-state current	$V_D = \text{rated } V_{DRM}$	$I_G = 0$	$T_C = 110^\circ\text{C}$			±2	mA
$I_{GTM}$ Peak gate trigger current	$V_{supply} = +12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		0.8	5	mA
	$V_{supply} = +12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		-4.5	-20	
	$V_{supply} = -12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		-3.5	-10	
	$V_{supply} = -12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		11.7	30	
$V_{GTM}$ Peak gate trigger voltage	$V_{supply} = +12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		0.7	2	V
	$V_{supply} = +12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		-0.7	-2	
	$V_{supply} = -12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		-0.8	-2	
	$V_{supply} = -12\text{ V}^\dagger$	$R_L = 10\ \Omega$	$t_{p(g)} > 20\ \mu\text{s}$		0.9	2	

† All voltages are with respect to Main Terminal 1.

## PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.

# TIC225 SERIES SILICON TRIACS

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## electrical characteristics at 25°C case temperature (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TM}$ Peak on-state voltage	$I_{TM} = \pm 12\text{ A}$ $I_G = 50\text{ mA}$ (see Note 6)		$\pm 1.6$	$\pm 2.1$	V
$I_H$ Holding current	$V_{supply} = +12\text{ V}\dagger$ $I_G = 0$ Init' $I_{TM} = 100\text{ mA}$ $V_{supply} = -12\text{ V}\dagger$ $I_G = 0$ Init' $I_{TM} = -100\text{ mA}$		3 -4.7	20 -20	mA
$I_L$ Latching current	$V_{supply} = +12\text{ V}\dagger$ (see Note 7) $V_{supply} = -12\text{ V}\dagger$			30 -30	mA
dv/dt Critical rate of rise of off-state voltage	$V_{DRM} = \text{Rated } V_{DRM}$ $I_G = 0$ $T_C = 110^\circ\text{C}$		$\pm 50$		V/ $\mu\text{s}$
dv/dt <sub>(c)</sub> Critical rise of commutation voltage	$V_{DRM} = \text{Rated } V_{DRM}$ $I_{TRM} = \pm 12\text{ A}$ $T_C = 70^\circ\text{C}$	$\pm 1$	$\pm 1.5$	$\pm 4.5$	V/ $\mu\text{s}$

† All voltages are with respect to Main Terminal 1.

NOTES: 6. This parameter must be measured using pulse techniques,  $t_p \leq 1\text{ ms}$ , duty cycle  $\leq 2\%$ . Voltage-sensing contacts separate from the current carrying contacts are located within 3.2 mm from the device body.

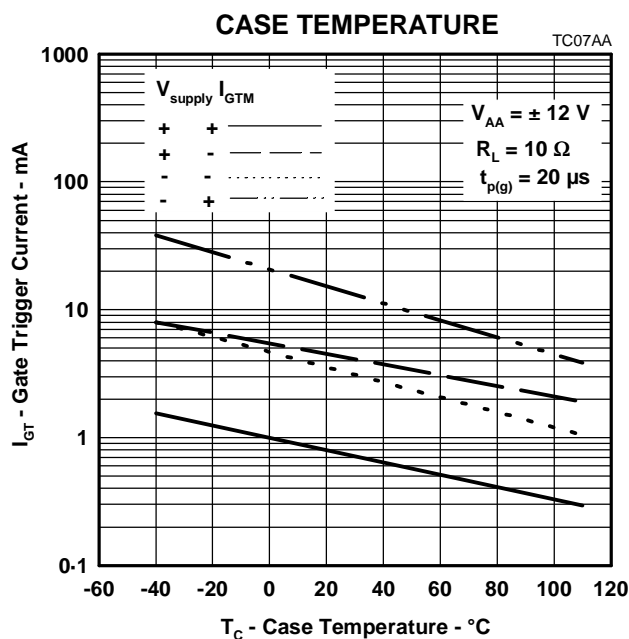
7. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics:  
 $R_G = 100\ \Omega$ ,  $t_{p(g)} = 20\ \mu\text{s}$ ,  $t_r \leq 15\ \text{ns}$ ,  $f = 1\ \text{kHz}$

## thermal characteristics

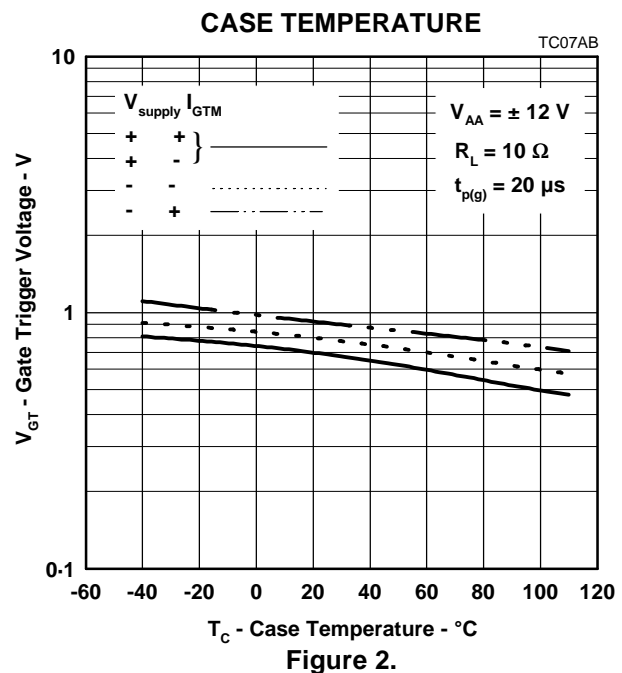
PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$ Junction to case thermal resistance			2.5	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction to free air thermal resistance			62.5	$^\circ\text{C/W}$

## TYPICAL CHARACTERISTICS

GATE TRIGGER CURRENT  
vs



GATE TRIGGER VOLTAGE  
vs



TYPICAL CHARACTERISTICS

HOLDING CURRENT  
vs  
CASE TEMPERATURE

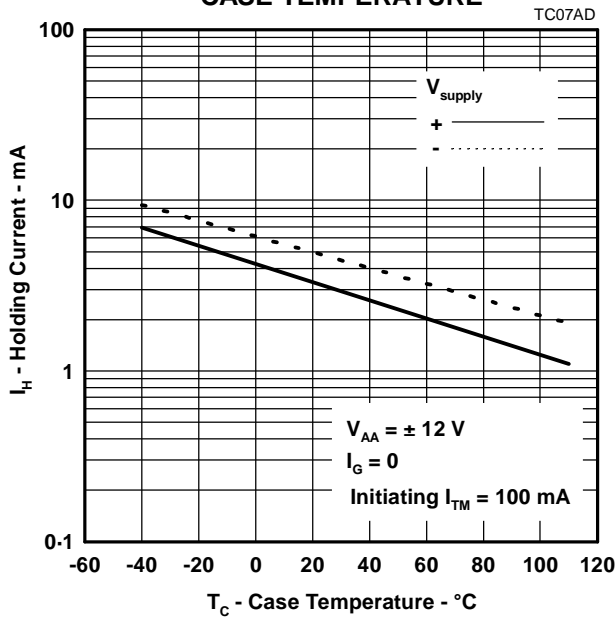


Figure 3.

GATE FORWARD VOLTAGE  
vs  
GATE FORWARD CURRENT

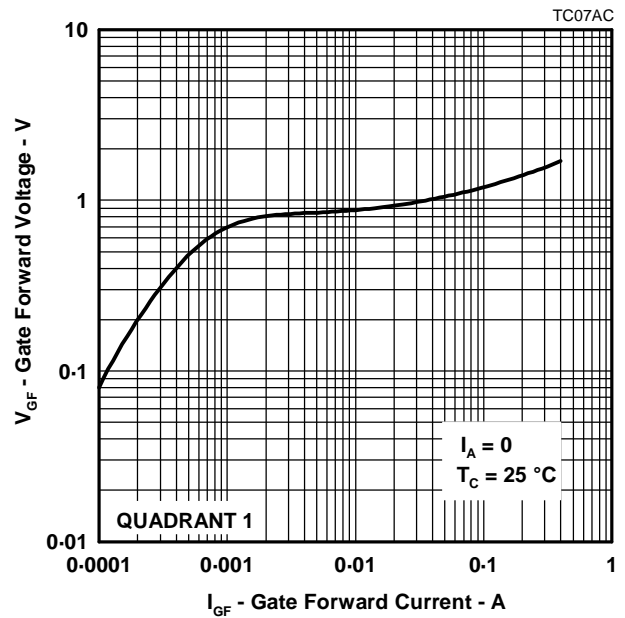


Figure 4.

LATCHING CURRENT  
vs  
CASE TEMPERATURE

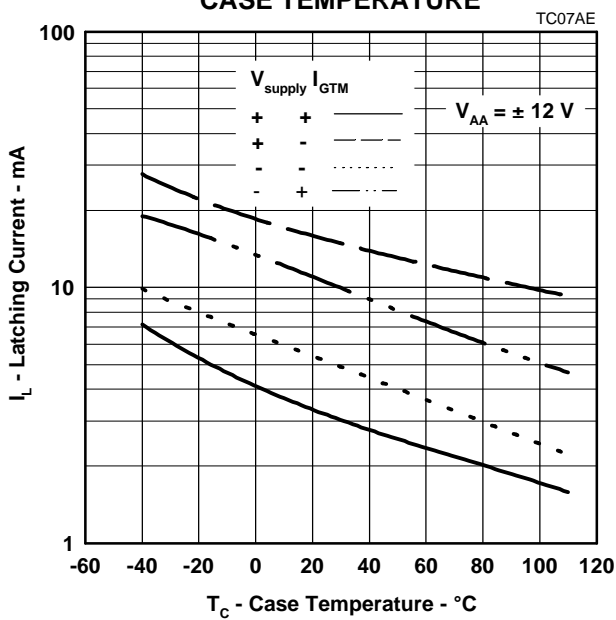


Figure 5.

SURGE ON-STATE CURRENT  
vs  
CYCLES OF CURRENT DURATION

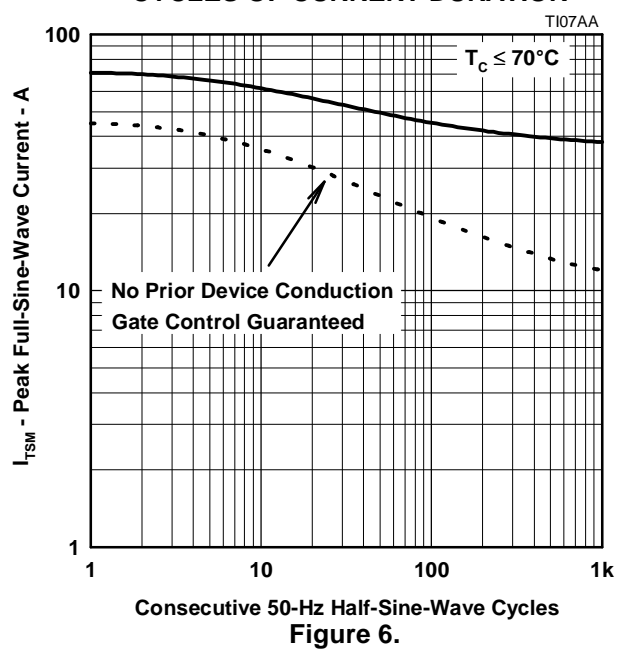


Figure 6.

# TIC225 SERIES SILICON TRIACS

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## TYPICAL CHARACTERISTICS

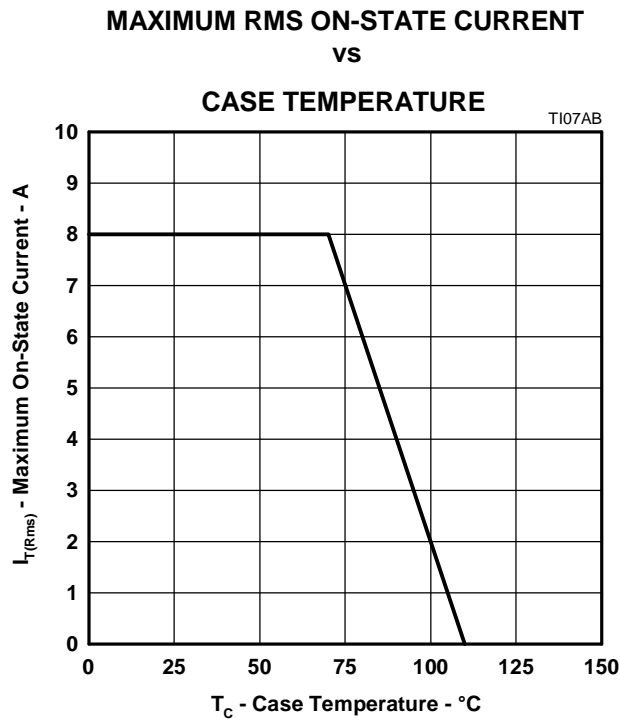
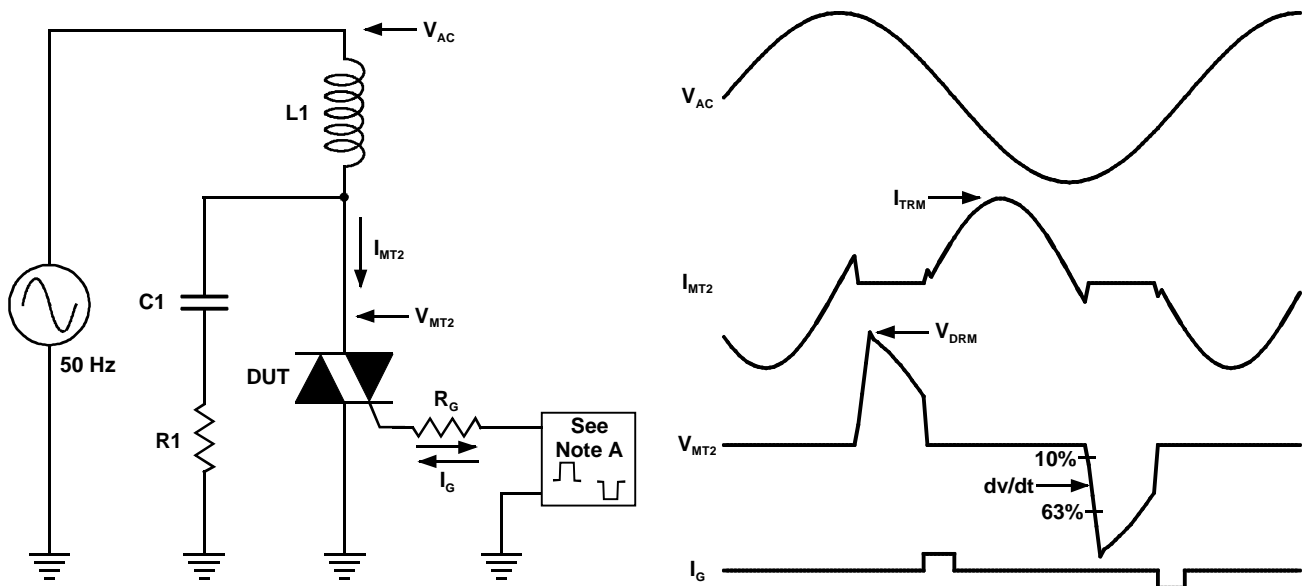


Figure 7.

## PARAMETER MEASUREMENT INFORMATION



NOTE A: The gate-current pulse is furnished by a trigger circuit which presents essentially an open circuit between pulses. The pulse is timed so that the off-state-voltage duration is approximately 800  $\mu$ s.

Figure 8.

PMC2AA

## PRODUCT INFORMATION

MECHANICAL DATA

TO-220

3-pin plastic flange-mount package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. The centre pin is in electrical contact with the mounting tab.  
 B. Mounting tab corner profile according to package version.  
 C. Typical fixing hole centre stand off height according to package version.  
 Version 1, 18.0 mm. Version 2, 17.6 mm.

MDXXBE

# TIC225 SERIES SILICON TRIACS

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