

# IRLIZ34NPbF

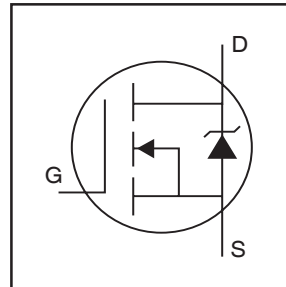
HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

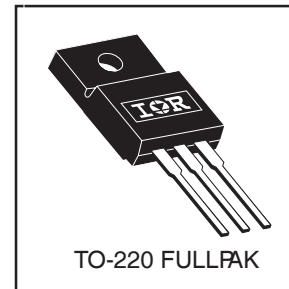
## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



$V_{DSS} = 55V$
$R_{DS(on)} = 0.035\Omega$
$I_D = 22A$



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	22	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	15	
$I_{DM}$	Pulsed Drain Current ④ ⑥	110	
$P_D @ T_C = 25^\circ C$	Power Dissipation	37	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy ② ⑥	110	mJ
$I_{AR}$	Avalanche Current ① ⑥	16	A
$E_{AR}$	Repetitive Avalanche Energy ① ⑥	3.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑥	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw.	10 lbf·in (1.1N·m)	

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	---	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	---	---	65	

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International  
**IR** Rectifier

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.065	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA⑥
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.035	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A ④
		—	—	0.046		V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 12A ④
		—	—	0.060		V <sub>GS</sub> = 4.0V, I <sub>D</sub> = 10A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	11	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 16A⑥
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	—	25	nC	I <sub>D</sub> = 16A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	5.2		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	14		V <sub>GS</sub> = 5.0V, See Fig. 6 and 13 ④⑥
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.9	—	ns	V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	100	—		I <sub>D</sub> = 16A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	29	—		R <sub>G</sub> = 6.5Ω, V <sub>GS</sub> = 5.0V
t <sub>f</sub>	Fall Time	—	21	—		R <sub>D</sub> = 1.8Ω, See Fig. 10 ④⑥
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	880	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	220	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	94	—		f = 1.0MHz, See Fig. 5⑥
C	Drain to Sink Capacitance	—	12	—		f = 1.0MHz

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	22	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	110		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 12A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	76	110	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 16A
Q <sub>rr</sub>	Reverse Recovery Charge	—	190	290	nC	di/dt = 100A/μs ④⑥

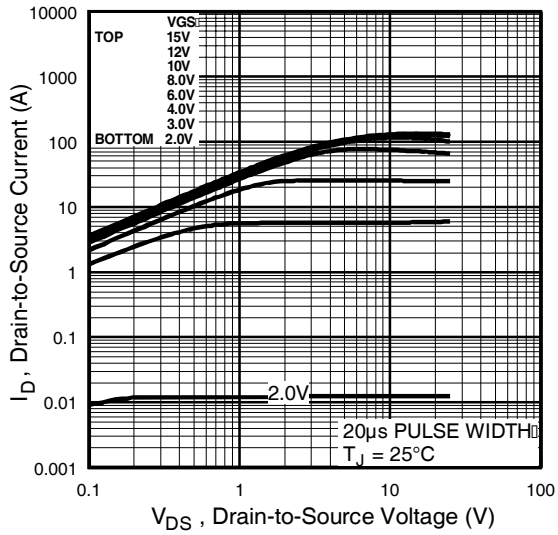
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )  
 ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 610μH  
 R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 16A. (See Figure 12)  
 ③ I<sub>SD</sub> ≤ 16A, di/dt ≤ 270A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
 T<sub>J</sub> ≤ 175°C

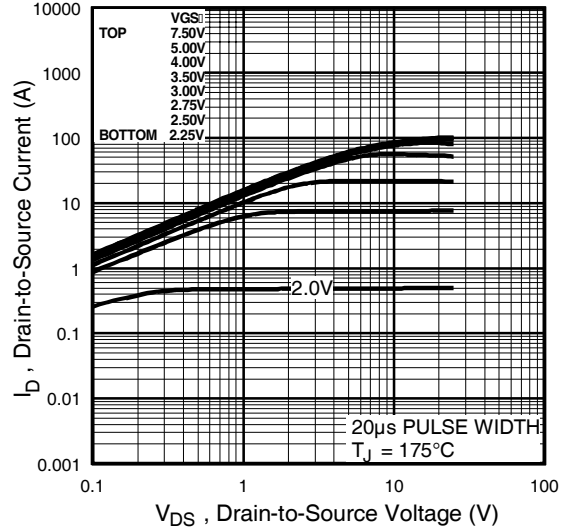
④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ t = 60s, f = 60Hz

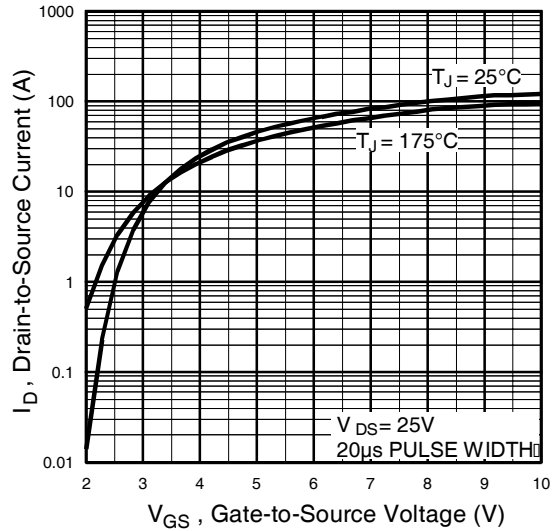
⑥ Uses IRLZ34N data and test conditions



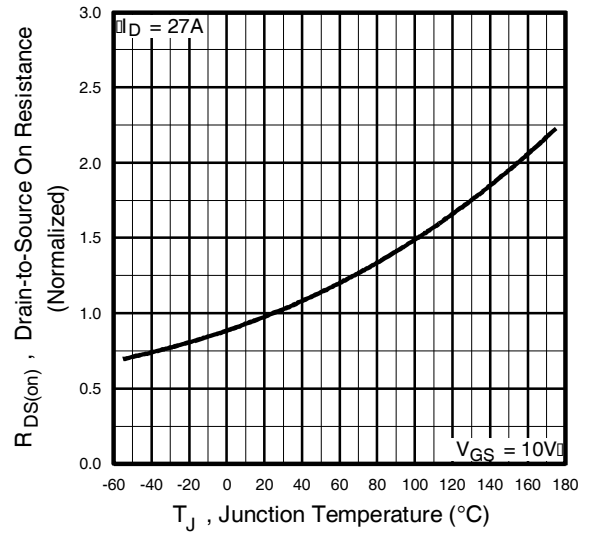
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

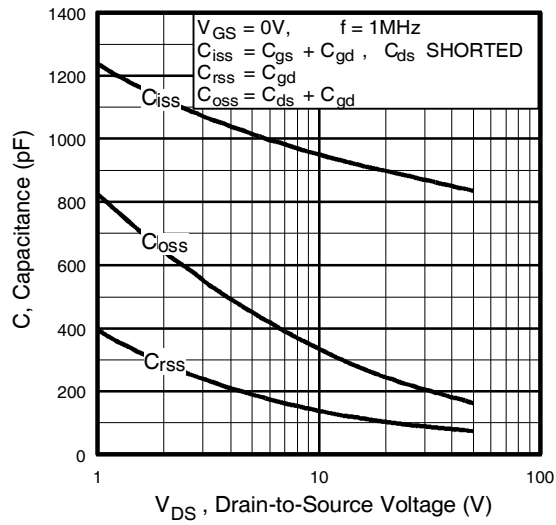


**Fig 3.** Typical Transfer Characteristics

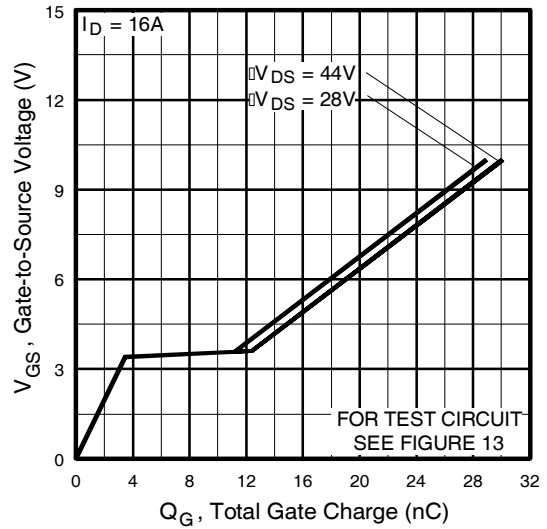


**Fig 4.** Normalized On-Resistance Vs. Temperature

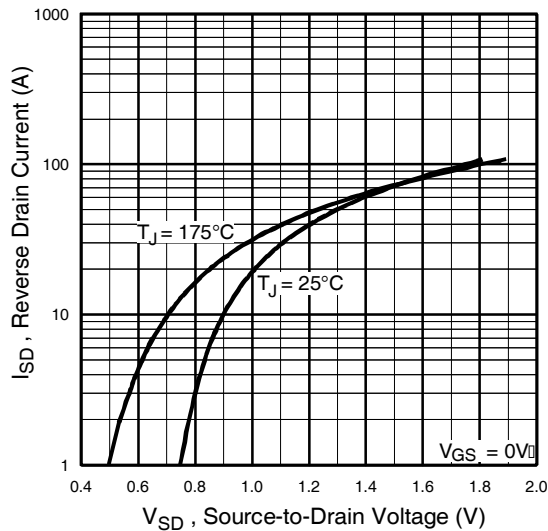
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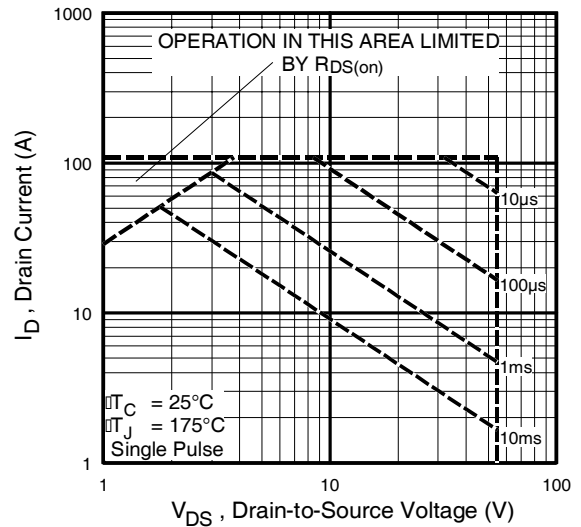
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



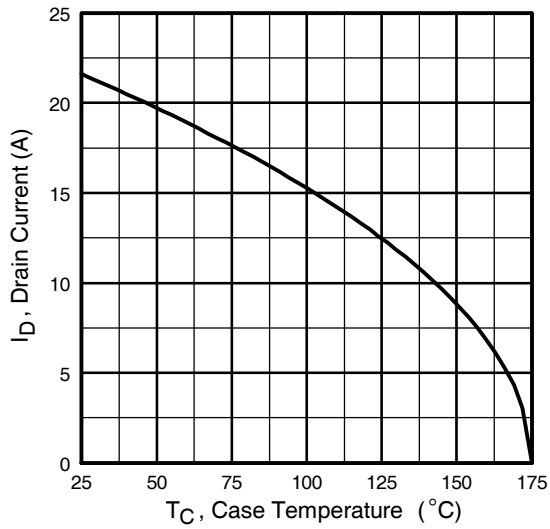
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



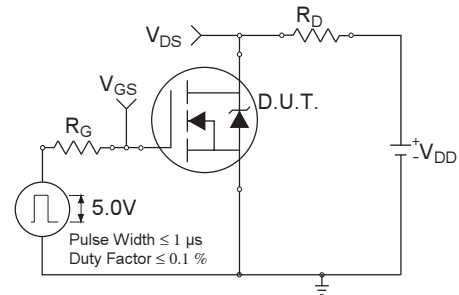
**Fig 7.** Typical Source-Drain Diode Forward Voltage



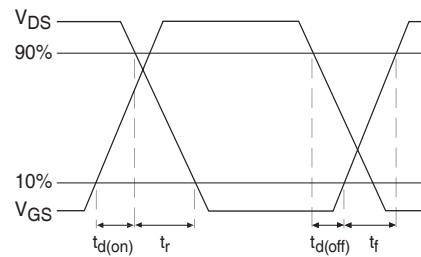
**Fig 8.** Maximum Safe Operating Area



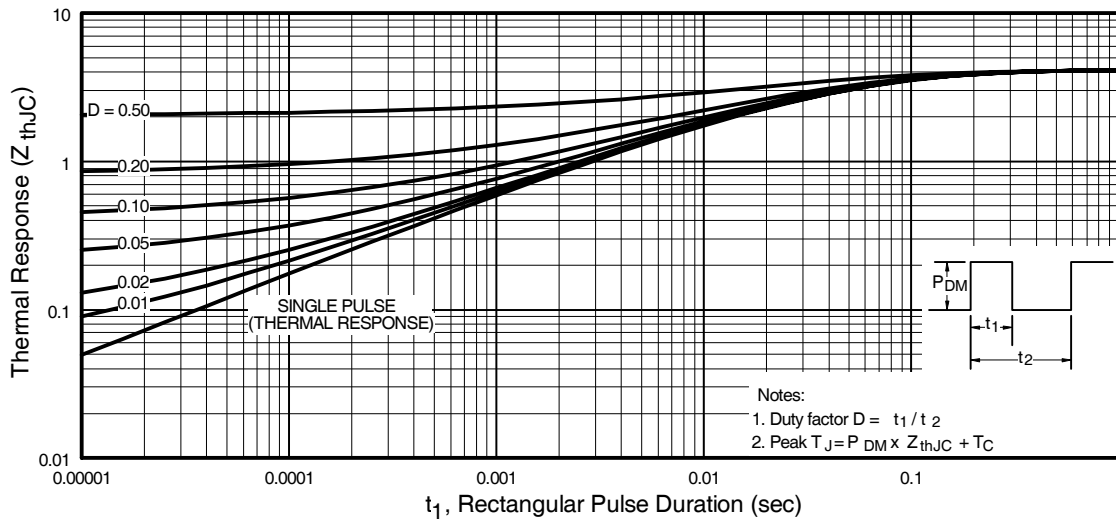
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



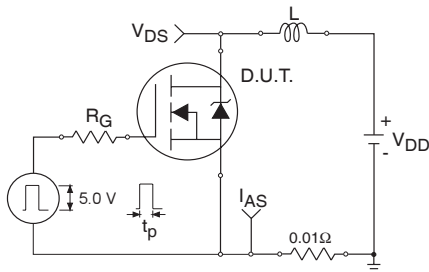
**Fig 10b.** Switching Time Waveforms



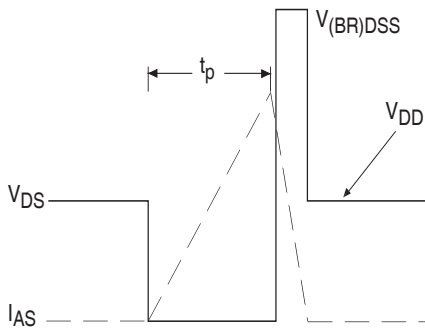
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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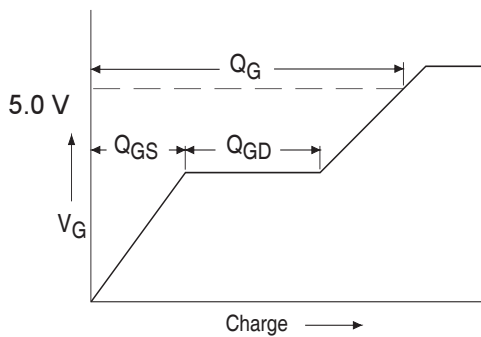
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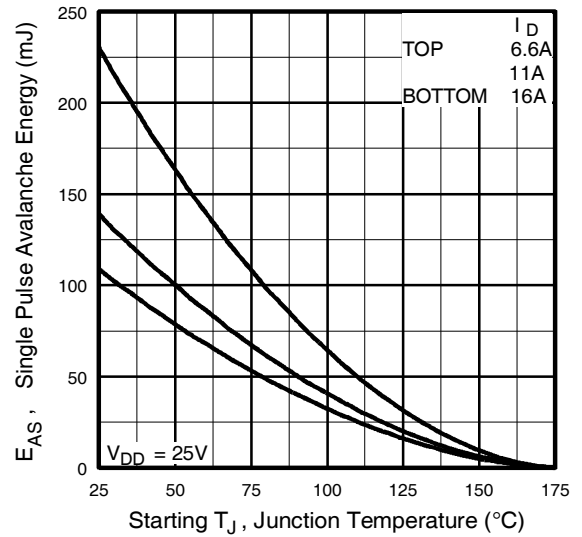
**Fig 12a.** Unclamped Inductive Test Circuit



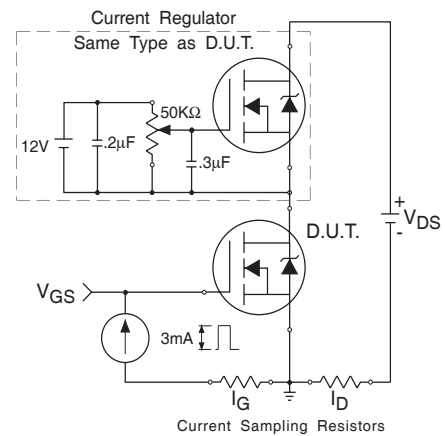
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

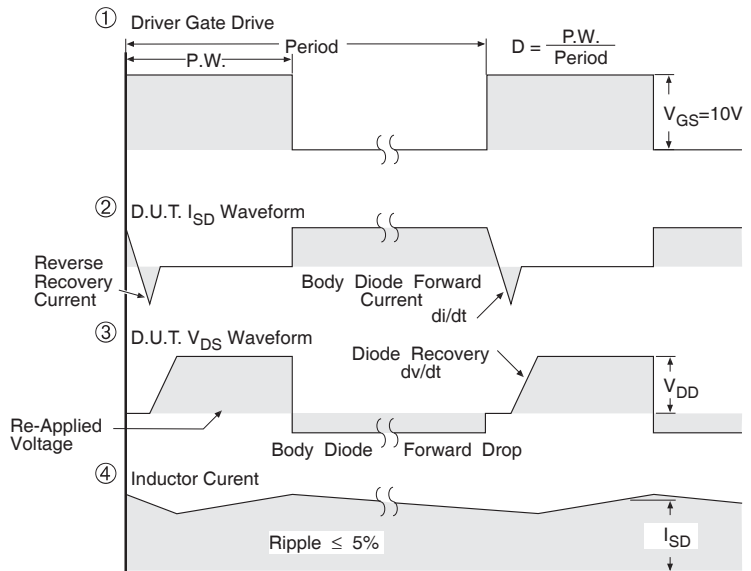
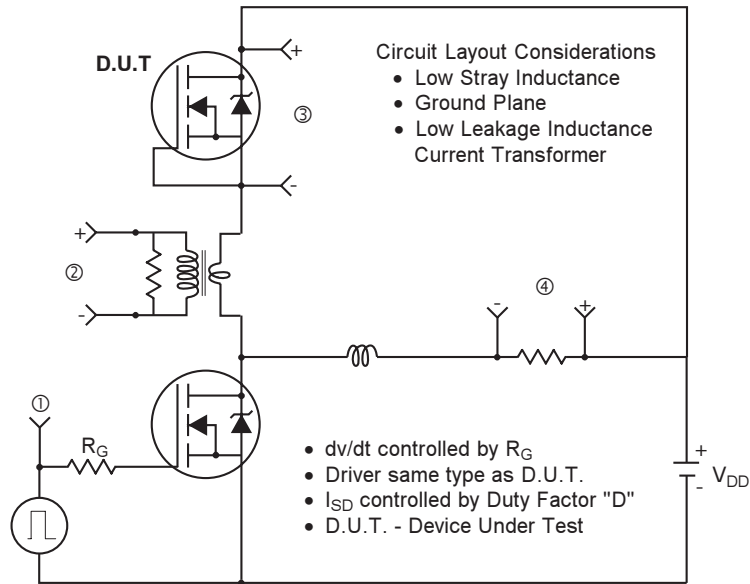


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

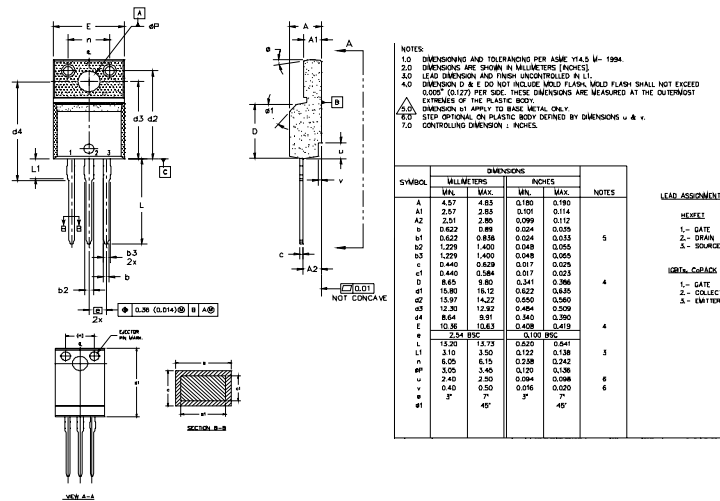
**Fig 14.** For N-Channel HEXFETS

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## TO-220 Full-Pak Package Outline

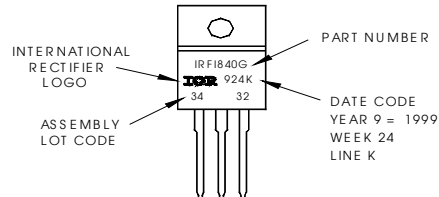
Dimensions are shown in millimeters (inches)



## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24 1999  
IN THE ASSEMBLY LINE "K"

**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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