MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD166
BD168
BD170

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

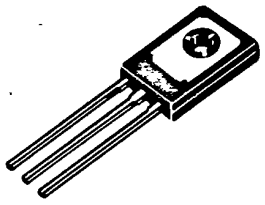
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 166, 168, 170 are complementary with BD 165, 167, 169

1.5 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
20 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	°C

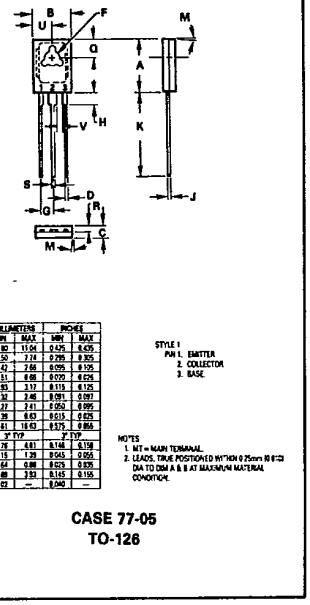
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD 166 BD 168 BD 170	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 166 BD 168 BD 170	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.92	11.04	0.430	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.80	3.17	0.110	0.125
G	2.30	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.88	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A, B & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

3

BD166, BD168, BD170

T-33-19

FIGURE 1 – P_D–T_C DERATING CURVE

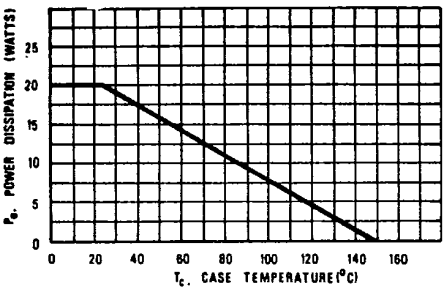
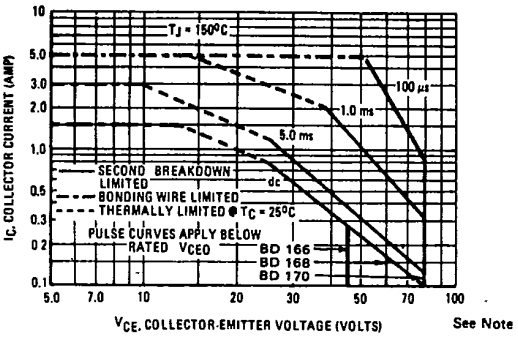


FIGURE 2 – SAFE OPERATING AREA



See Note

FIGURE 3 – COLLECTOR SATURATION REGION

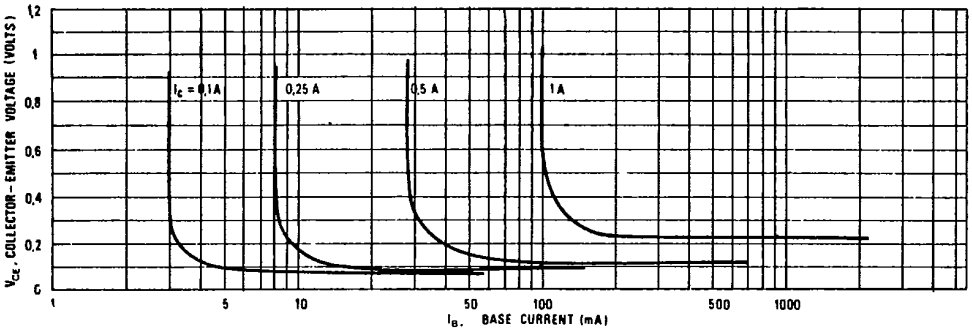


FIGURE 4 – CURRENT GAIN

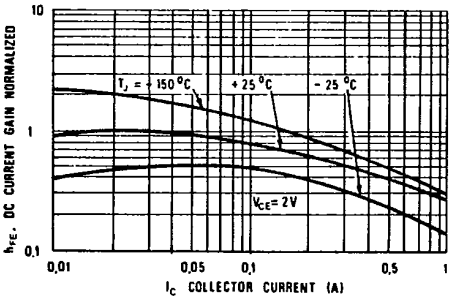
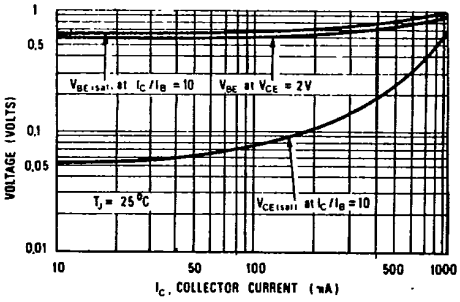


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)